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3D Sequential Integration via Direct Bonding of Highly Conductive Sputtered Tungsten Films

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Abstract

To further extend CMOS road map, a great interest has been sparked in the development of 3D sequential integration. In this new integration scheme, the question of inter-level connections is left open. So far the only available option lies on direct bonding of dielectric films and subsequent metal contact formation. Here we suggest an alternative cold integration route where the Smart Cut™ technology is performed via direct bonding of sputtered tungsten films. In this regard, the involved metal layers not only ensure 3D assembly but also provide a frame for inter-level connection, reducing significantly upper level congestion. To bond a refractory material at low temperatures (<400 °C), we carried out a controlled passivation and took advantage of its instability to achieve a sealing throughout crystallization. This approach is ideal for the integration of high-performance logic units with nonvolatile memories and opens up the possibility of multiple iterations by thinking ahead inter-level connections.

1. Introduction

Thanks to its high alignment precision (< 10 nm), 3D sequential integration is the only technological option that takes full benefits of the third dimension [1]. When associated to Solid Phase Epitaxial Regrowth (SPER), the Smart Cut™ technology, which combines ion slicing and direct bonding, has recently proven to be a reliable sub-500 °C method to ensure the layer transfer of high quality single crystal silicon films with proper electrical properties on top of a processed wafer [2]. In this paper, we explore a variation of the above mentioned technology. As depicted in figure 1, the idea here is to take advantage of metal bonding to grant a strong mechanical and electrical link between active levels and reduce even more interconnection length for increased overall performances [3].

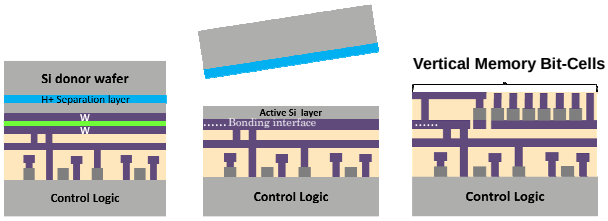

Fig. 1: The Smart Cut™ technology based on metal bonding for 3D integration of logic control units with nonvolatile memories.

Within these integration levels and scales the list of suitable materials to serve as conductive bonding layers is limited. Because of a poor conductivity or a high formation temperature, silicides do not meet the requirements of such integrations. The best candidate must be found among metals. In this regard, tungsten, with the highest melting point, appears as the most promising candidate for at least four reasons: (I) a low diffusivity in silicon at temperatures below 400 °C resulting in a very low contamination potential; (II) a high stability and reliability meaning limited electromigration and associated failures; (III) a thermal expansion coefficient around $4.8 \cdot 10^{-6}.K^{-1}$ making it sparsely prone to stress-induced voiding; (IV) finally a small electronic free mean path (EFMP) making it an even better conductive material than copper when connection line widths are below 39 nm [5-6].

However, because of its unique properties, W is a very difficult material to bond via a diffusion activated mechanism from room temperature (RT) to 400 °C. In addition, because bonding is performed in ambient air, surface native oxide management becomes crucial to obtain a robust conductive assembly [7], especially in the case of W where various oxide phases are involved with different composition and thermal stability [8]. To overcome these difficulties, we focused on Physical Vapor Deposition (PVD) technique to form specific W bonding layers. In the first place because PVD produces W layers of higher purity and greater electrical properties than other techniques [4] and most importantly because PVD offers the possibility to control the formation of a top passivating tungsten oxide (WO_x) by incorporating different amounts of oxygen in the sputtering deposition plasma. Thanks to this approach, we managed to identify a specific passivation which, despite its instability with temperature, shows a favorable evolution during post bonding annealing process. As a first proof of concept and in order to demonstrate our approach in the 3D sequential integration context, we focused our efforts on the realization of a sub-400 °C Si layer transfer via the bonding of 10 nm-thick passivated W layers.

2. Experimental and Results

Deposition

All wafers used in the study are p-type 200 mm Si-(100) blanket wafers. A bilayer structure composed of 10 nm-thick W followed by a 5 nm-thick WO_x layer is deposited on top of a SiO_2 layer. All depositions were performed in a magnetron sputtering system at temperatures below 40 °C (confirmed by sensitive stickers) and under vacuum below 2.10^{-7} Torr. Argon pressure was fixed. Regarding the reactive sputtering process resulting in WO_x formation, the amount of incorporated oxygen was regulated by the flow-rate R defined as the ratio of oxygen flow-rate to the sum of oxygen and argon flow-rates. A wide range of R was explored. For the sake of clarity, we limited the results to the most interesting cases: R = 0% (reference case resulting in the formation of a native oxide when exposed to air), 15 % and 25 % (controlled passivation).

The morphology of these layers was inspected by Atomic Force Microscopy (AFM): the 0 % case exhibits small grains, a classical signature of the columnar structure of W layers. For R = 15 % and 25 % the footprint is more of an amorphous state. These structural properties were confirmed by X-Ray Diffraction (XRD) as shown in figure 2.

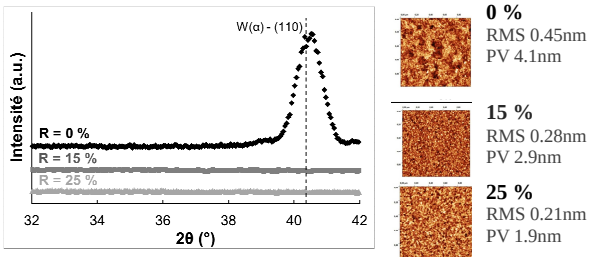

Fig. 2: XRD characterization and 1 x 1 µm² AFM scans of passivated W layers according to the flow rate ratio R.

Measured thicknesses and densities measured by X-Ray Reflectivity (XRR) are reported in table 1. The reference at R = 0 % has a thin native oxide layer with a density between WO_2 and WO_3 (respectively established at 10.8 and 7.16 g.cm^{-3}) while other conditions exhibit different density values which are lower than WO_3. These characterizations confirm that a controlled passivation significantly differ from a native oxide.

Table I. Thickness and density of WO_x measured by XRR

R	0 % (native oxide)	15 %	25 %
Thickness(nm)	1.1	5.4	5.1
Density (g.cm^{-3})	8.4	6.2	6.0

Bonding

Wafer level WO_x-WO_x direct bonding was performed at RT and ambient air without extra preparation. Bonding evolution with temperature was monitored via Scanning Acoustic Microscopy (SAM) and toughness was estimated by double cantilever beam (DCB) method under prescribed displacement [9].

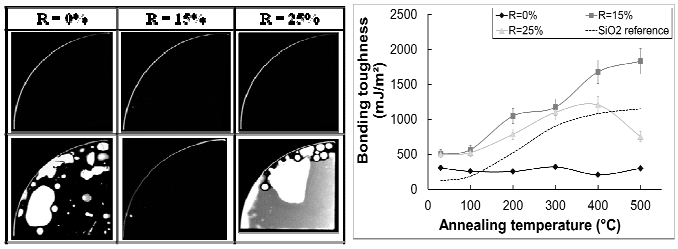

Fig. 3: Temperature evolution of bonded structures involving W and WO_x layers via SAM (defects appear in white) and DCB characterizations.

In good agreement with literature [7], the reference bonding (R = 0 %) has a poor bonding adherence as it could be observed on figure 3. Both controlled passivation (R = 15 and 25 %) show a better evolution than native WO_x or traditional SiO_2 bonding. Nevertheless in the case of R = 25 % the apparition of bonding defects leads to a drop of toughness between 400°C and 500°C. A very interesting behavior is shown by the case R = 15 %.

Layer transfer

In order to achieve the layer transfer, one of the substrate (called donor) was ion-implanted with hydrogen before metallization. A similar bilayer structure W and WO_x is formed on both wafers which were directly bonded. In the light of our previous results, the flow-rate ratio R was set at 15 %. The bonded structure was annealed until the splitting temperature between 300 and 400 °C. Bonding layer morphology was inspected by Transmission Electron Microscopy (TEM).

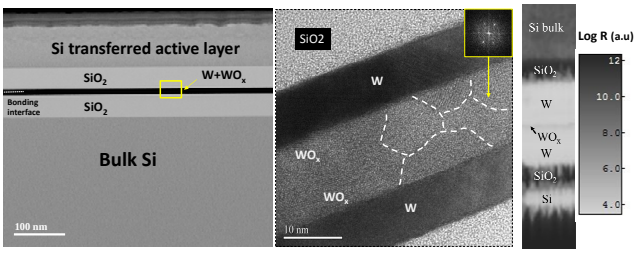

Fig. 4: TEM cross-section: low (left) and high magnification (center) images of a thin Si film transferred via W-WO_x bonding, (Right) 2D relative resistance map of the cross section.

After annealing, the original bonding interface is no longer observable and only one rebuilt and crystalized WO_x layer is observed. Prior to bonding, the resistivity of sputtered W layers was measured (via four probe technique) at 17.5 µΩ.cm (bulk value is 5.3 µΩ.cm [4]). The electrical properties in the bonded structure were assessed by Scanning Spreading Resistance Microscopy (SSRM) technique. As shown in figure 4, the relative resistance rise at the bonding interface remains barely noticeable. Ongoing measurements on Kelvin cross structures should refine this result with quantitative measurements.

Conclusions

We took advantage of PVD technique to passivate high quality W layers. In specific conditions, we formed instable and amorphous layers ready for RT bonding. These layers have a favorable evolution with temperature, resulting in a complete crystallization of the bonding interface. This sub-400 °C process is a credible alternative to traditional SiO_2 bonding allowing both vertical electrical connection and 3D assembly via layer transfer.

Acknowledgements

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