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Reliability Results of 4 million Micro Bump Interconnections of 3D Stacked 16 M Pixel Image Sensor

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Abstract

We evaluated the reliability of 3D stacked CMOS image sensors (CISs) with 4 million micro bump interconnections at a 7.6-um pitch bonded with wafer bonding technology. This 3D stacked technology was proved to have no negative effect on CIS characteristics and to provide a high density and narrow pitched in-pixel connection with high reliability, no defects, and no deteriorations over a 1000-cycle heat cycle test and 1000-hour high temperature and high humidity test. This CIS sensor has a set of readout circuits in each substrate, which enable us to detect any connection failure among 4 million micro bumps between substrates individually. These results show that this 3D technology has enough reliability for application to products.

1. Introduction

As we previously proposed [1], introducing 3D stacking technologies to image sensors gives them more functionality and improves their performance [2]. A CMOS image sensor (CIS) with a global shutter function is ideal for digital cameras because it is free from distortion when capturing a moving target, but it needs an extra in-pixel storage node. The parasitic light sensitivity of an in-pixel storage node must be less than one hundred millionth of that of a photodiode (PD) to prevent artifacts, which is almost impossible except with a 3D pixel with connected storage node in another substrate to protect from not just incident light but also photo-generated carriers. Through-silicon via (TSV) technology, however, is not applicable to such global shutter CISs as an in-pixel interconnection is required to connect storage nodes. This micro bump interconnection technology solves these problems and is the most advanced 3D technology in terms of number and pitch [4, 5].

In this work, we evaluated electric interconnections between substrates and resistance variations of the micro bumps during reliability tests in massive numbers, 4 million per chip. We confirmed that the micro bump interconnections endure a heat cycle test and high temperature and high humidity test.

2. Structures

Figure 1 shows a schematic of our CIS, which is composed of two substrates. The top substrate has a PD array with 3.8-μm pixels, vertical scanning circuits, and readout circuits. The bottom one has a storage node array, vertical scanning circuits, and readout circuits. PDs and storage nodes are electrically connected through a micro bump at a 7.6-μm pitch, as shown in Fig. 2. The chip size is 20.42 × 19.98 mm, applicable to micro four thirds cameras. Both the bottom and top substrates have their own vertical scanning circuits and readout circuits, which enables two modes, Hybrid mode and Monolithic mode, shown in Fig. 3. The signals are read out through micro bumps in Hybrid mode. In Monolithic mode, each photo diode signal is read out in the top substrate by itself. Comparing measured data enables us to distinguish micro bump interconnection defects from other defects and to monitor a huge number of interconnections, as many as 4 million per chip.

Test Element Group (TEG) chips were used as tools to check precise changes in the resistance of a micro bump interconnection. Figure 4 shows a schematic of the TEG, whose resistance consisted of a micro bump and the base of the micro bump and was measured with a four-terminal method.

3. Experiment

3D stacked devices, which generally consist of materials with different thermal expansion coefficients, tend to be so vulnerable to temperature changes that it is most important and critical for them to be robust when applying them to products. We conducted heat cycle tests with CIS and TEG chips and high temperature and high humidity tests with TEG chips.

The heat cycle test condition for the CIS chips was -40 to 85°C every 30 minutes for 1000 cycles. The heat cycle test condition for the TEG chips was 105 and -40°C every 30 minutes for 1000 cycles.

The high-temperature and high-humidity test condition for the TEG chips was 85°C and 85% for 1023 hours.

4. Results

Figure 5 shows the defect rate vs. test time in the heat cycle test, in which five CIS chips with a total of 20 million bump interconnections were tested. The defect rate of the interconnections did not increase over the test time. This means that this 3D interconnection has enough reliability and durability for practical use. Furthermore, we conducted

the same test with the TEG chips to measure the changes in resistance of the interconnections with high accuracy. The results of the heat cycle test with the TEG chips are shown in Fig. 6. The changes were less than 10% for 1000 cycles. Considering the original resistance and interconnection performance, this means no changes were observed, so this micro bump interconnection, we think, has enough reliability for application to products.

Figure 7 shows the results of the high temperature and high humidity test with the TEG chips. The changes were less than 50% for 1023 hours. The original interconnection resistance was so small, a few mΩ, that the fluctuation range looked very large, but no deteriorations were observed.

5. Conclusion

We tested the reliability of 3D stacked CMOS image sensors with 4 million micro bump interconnections at a 7.6-um pitch bonded with wafer bonding technology. In the tests mode, we scanned 4 million micro bump interconnections per chip to distinguish interconnection failures from the others. In heat cycle tests with CIS and TEG chips and high temperature and high humidity tests with TEG chips, this 3D stacked technology was proved to provide a narrow pitched in-pixel connection with high reliability, no defects, and no deteriorations over a 1000-cycle heat cycle test and 1000-hour high temperature and high humidity test. The results show that this 3D technology has high interconnection yields and satisfactory reliability for use in our products.

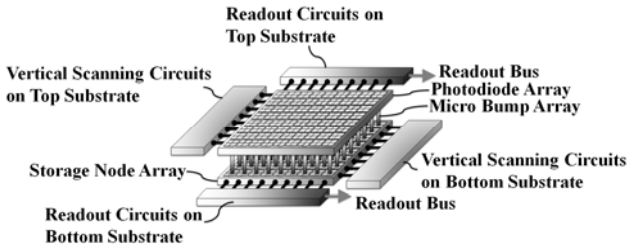

Fig. 1 Schematic of our CIS chip

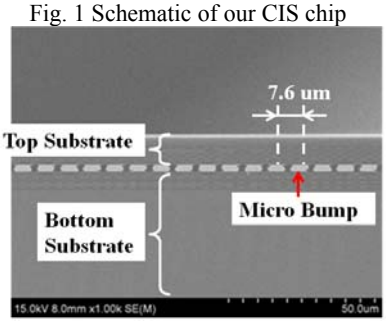

Fig. 2 Cross-sectional image of our CIS chip

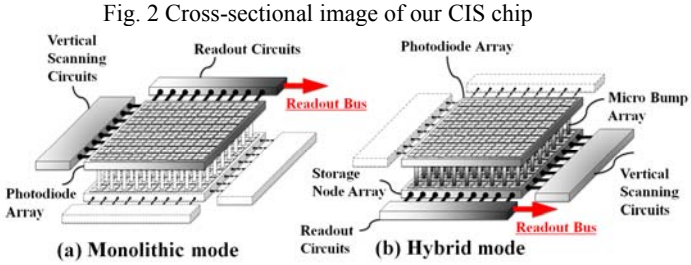

Fig. 3 Schematic of two modes

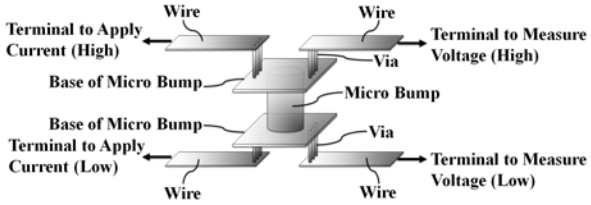

Fig. 4 Schematic of TEG chip

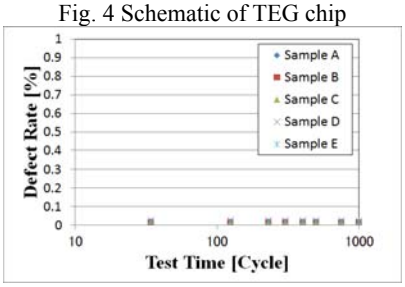

Fig. 5 Number of defective bumps vs. test time in heat cycle test with CIS

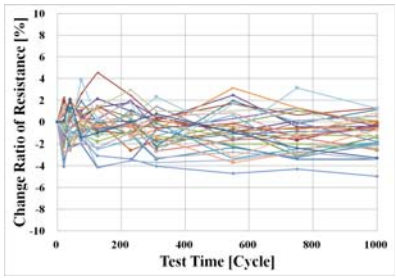

Fig. 6 Change ratio of micro bump interconnection resistance vs. test time in heat cycle test with 31 TEGs

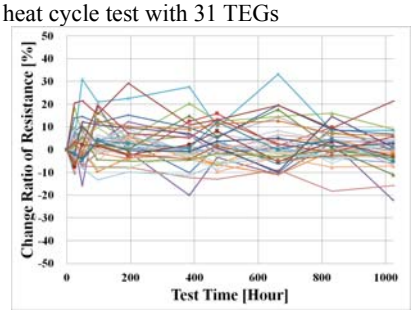

Fig. 7 Change ratio of micro bump interconnection resistance vs. test time in high temperature and high humidity tests with 38 TEGs

References

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