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# Evaluation of 2-D Local Stress Distribution in Stacked IC Chip Using Stress-induced Retention Time Modulation of DRAM Cell Array

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**Abstract**

Stacked IC technology using a lot of through-Si vias (TSVs) has been used for enhancement of IC performance. Stacked ICs are mechanically connected by metal bumps and organic adhesive injected among stacked chips. However, Coefficient of thermal expansion (CTE) mismatch between metal bumps and organic adhesive will induce local bending in stacked IC chips, which causes negative effects to transistor performance. In this study, we evaluated a relationship between 2-dimensionally (2-D) local bending stress distribution and retention characteristics of DRAM cell array with planar MOS capacitors in the stacked IC chip. Consequently, we have successfully clarified the effects of the 2-D local bending stress distribution on electrical characteristics even in the stacked thick IC chips. Using the DRAM cell array with planar MOS capacitors for the local bending stress evaluation, appropriate design guidelines for the stacked IC can be developed and various kinds of stacked ICs will be realized with high performance and high reliability.

## 1. Introduction

Stacked IC technology with lots of TSVs is one of the promising technologies for IC performance enhancement. In the stacked IC, each chip is mechanically connected by metal bumps and organic adhesive. The CTE of organic adhesive is almost larger than that of metal bumps, which induces 2-dimensionally-distributed local bending stress in thin IC chips [1] and resultant carrier mobility modulation [2, 3]. However, there is not a method to precisely evaluate effects of the 2-D local bending stress distribution on electrical characteristics of electron devices fabricated in the stacked ICs. Therefore, a novel evaluation method is strongly required to quantitatively clarify relationships between the 2-D local bending stress distribution and device performances.

It is well-known that early DRAM has a planar MOS capacitor, where capacitor charges are supplied from source/drain region and Si substrate as shown in Fig. 1. As carrier mobility and number of carrier are modulated by substrate bending stress [4], it is possible to estimate the 2-D local bending stress in the stacked ICs by retention time modulations of the DRAM cell array with planar MOS capacitors. In this paper, a new technology is proposed to evaluate the 2-D local bending stress distribution using stress-induced retention time modulation of DRAM cell array.

## 2. Experiment

The test structure is composed of the DRAM cell array chip with MOS capacitors and a Si interposer. Figure 2 shows a photograph and a layout of the DRAM chip with Cu/Sn bump. The DRAM chip was fabricated by 90-nm standard CMOS technology and has 40 macros where each macro has 8kbit memory cells. There were various kinds of bump sizes and pitches for inducing different local bending stresses. Figure 3 shows a fabrication process flow. The DRAM chip was 200μm thick, and was bonded on the Si interposer with Cu/Sn bumps at 280°C for 420sec. Epoxy was injected between the DRAM chip and Si interposer, and cured at 150°C for 30min. Figure 4 shows a fabricated test structure with DRAM chip bonded on the Si interposer. In this paper, both retention time and backside surface profile of 11$^{th}$ macro in the DRAM cell array were measured. In the 11$^{th}$ macro, the size and pitch of Cu/Sn bump were 80 x 20μm and 220μm, respectively.

## 3. Results and Discussion

Figure 5 shows the measurement results of a backside surface curvature along X-position of the 11$^{th}$ macro at Y-position of 0.045mm after under-filling, and also shows a 2-D mapping of the retention time modulation caused by under-filling in the same macro. The curvature was calculated by the backside surface profile of DRAM-chip. In general, the curvature is proportional to the local bending stress. The retention time modulation was determined by time changes from initial retention time for each cells. As results, a pitch of convex positions in the curvature was 220μm, which was approximately the same as bump pitch. The retention time also clearly increased at every convex position, that was, above the Cu/Sn bumps. Therefore, it is

concluded that the 2-D mapping result of retention time modulation of DRAM cell array with planar MOS capacitor obviously indicated the 2-D local bending stress distribution.

## 4. Conclusion

A new method was proposed to evaluate a 2-D relationship between the local bending stress and retention characteristics of DRAM cell array with planar MOS capacitors. The DRAM cell array chip was bonded on the Si interposer to induce the 2-D local bending stress distribution due to the CTE mismatch between the organic adhesive and Cu/Sn bumps. The retention time modulations were coincident with backside surface curvatures of the DRAM chip. As results, it was successfully clarified that the local bending stress affected electrical characteristics of the device even in the thick IC chips. Using our proposed method, optimized design guidelines for the stacked IC can be developed and various kinds of stacked ICs will be realized with high performance and high reliability.

## References


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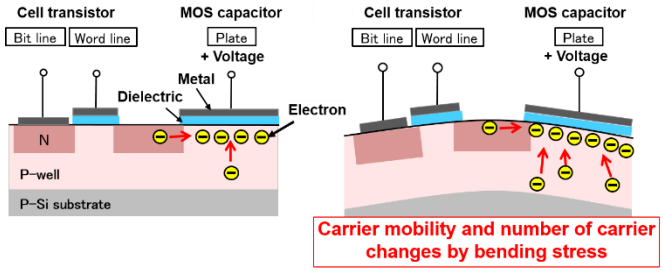
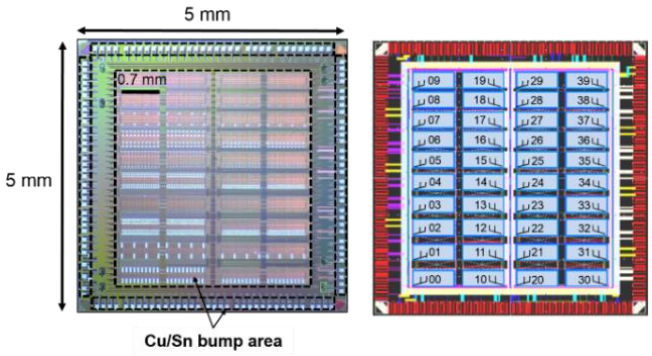



(a) (b)

Fig. 1. Schematic drawings of carrier behaviors in DRAM cell with planar MOS capacitor (a) without and (b) with bending stress.




(a) (b)

Fig. 2. (a) Photograph and (b) layout of the DRAM chip with Cu/Sn bump.

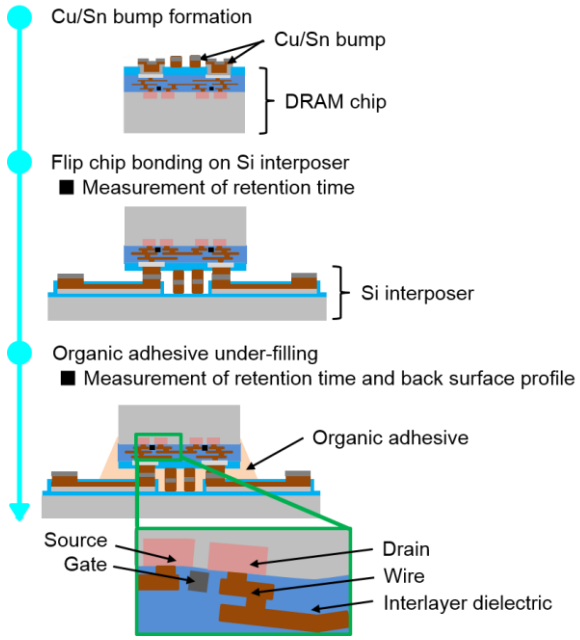



Fig. 3. Fabrication process of the DRAM chip bonded on the Si interposer.

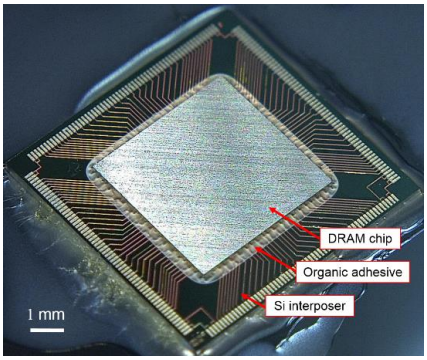



Fig. 4. Photograph of the fabricated DRAM chip bonded on the Si interposer.

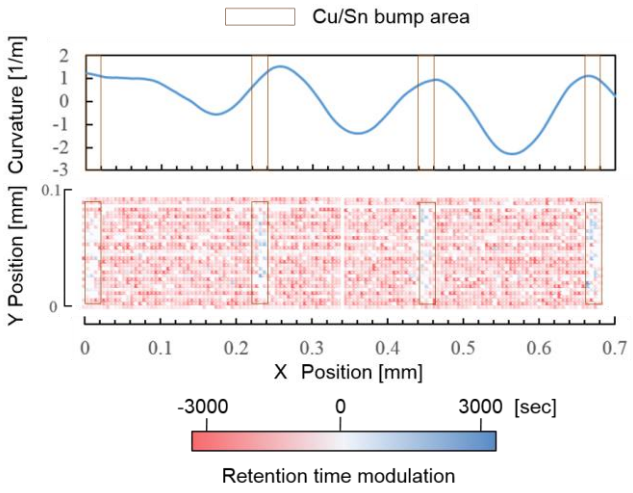



Fig. 5. Backside surface curvature along X-position of the DRAM chip after under-filling at Y-position of 0.045mm and 2-D mapping of the retention time modulation caused by under-filling in the 11th macro of DRAM cell array.