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Novel Integration of Ultra-thin Al_2O_3 with Low-*k* Dielectric as Bi-layer Liner for Capacitance Optimization and Stress Mitigation in Cu-TSV

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Abstract

A bi-layer liner is integrated in Cu-TSV for capacitance optimization and stress mitigation. Low-*k* (SiOC) liner with smaller elastic modulus is integrated in TSV and lower stress is exerted on the surrounding Si compared with PETEOS. It also reduces the TSV capacitance by ~26%. Thin Al_2O_3 is inserted between low-*k* liner and Si substrate to induce negative fixed charge (Q_f = -1.3 × 10^{12}cm^{-2}). This causes flat-band voltage shift (ΔV_{FB} = +19V) and the TSV is operated in the stable accumulation region hence immune to spatial variation due to hot-spot heating.

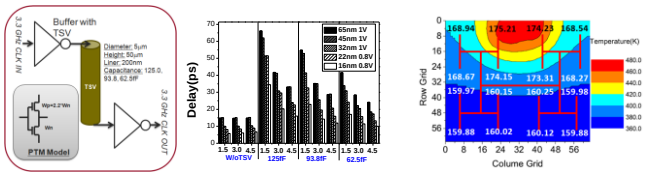
1. Introduction

TSV allows "orthogonal scaling" in the next generation of integrated circuits and systems for performance growth and functional diversification. TSV is fabricated by deep silicon etching, lining with dielectric and filing with Cu [1] hence forming a MOS structure [2]. Cu-TSV exerts thermo-mechanical stress on Si due to CTE mismatch which results in mobility variation [3] and interconnect distortion [4]. In addition, TSV parasitic capacitance has predominant impact on the circuit operation [5]. The depletion capacitance (C_{dep}) is susceptible to and increases with temperature. The fluctuation in C_{dep} and the impact on TSV signal delay is calculated using a predictive technology model (PTM) in Fig. 1(a)(b). When TSV is operated in the depletion region (~ 0-5 V), C_{dep} dependence on temperature results in spatial TSV latency variation and clock skew in H-tree network in the event of non-uniform hot-spot heating (Fig. 1(c)). Therefore, TSV with tolerance to spatial variation is desirable for robust 3DIC design. TSV capacitance is stable with temperature if one operates it in the accumulation region (C_{ox}). As C_{ox} is higher than C_{dep}, one needs to keep the capacitance <100 fF for final application [6].

One solution to TSV stress and capacitance issues is to use low-*k* dielectric liner with lower elastic modulus [7] and permittivity [8]. Flat-band voltage (V_{FB}) shift is achieved by including negative fixed charge at the *p*-Si/liner interface with a thin layer of Al_2O_3 such that the TSV operates at stable C_{ox} [9]. In this paper, we are presenting this novel integration of ultra-thin Al_2O_3 with low-*k* dielectric as bi-layer liner in Cu-TSV.

2. TSV Fabrication

Three sets of TSV structures (ϕ=5μm, aspect ratio =1:3) are fabricated on 8" *p*-Si wafer. This aspect ratio is chosen for ease of fabrication and is sufficient to study the properties of the liner. The TSV fabrication process is similar to that reported in [10]. Thin Al_2O_3 layer (~10 nm) is deposited in one set of TSV structures by atomic layer deposition (ALD) process at a temperature <400℃, followed by a Black Diamond low-*k* liner (~200 nm) deposition which is carried out in a PECVD chamber at 350 ℃. Hence the bi-layer liner is formed. The other two sets of TSV structures have PETEOS liner (~200 nm) deposited at 400 ℃ and Black Diamond low-*κ* liner (~200 nm) deposited, respectively, as control samples.



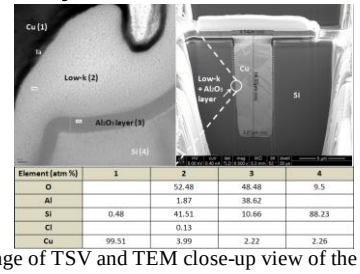
(a) (b) (c)

Fig.1. (a) TSV signal delay estimation using predictive technology model (PTM) for different capacitance; **(b)** Comparison of TSV signal delay for different technology node, *n*-MOSFET width (W_n in μm) and TSV capacitance (fF); **(c)** H-tree clock skew (ps) due to non-uniform hot-spot heating and the corresponding spatial variation in TSV capacitance.

3. Results and Discussion

Fabrication Process Results

A void-free Cu filled TSV with a combination of Al_2O_3 and low-*k* bi-layer liner is shown in Fig. 2. TEM and EDX analysis result in Fig. 2 show the chemical composition of Si, Al_2O_3, low-*k* and Cu, and also confirms that the Al_2O_3/low-*k* bi-layer is successfully and conformally integrated as the TSV liner with an average thickness of ~200 nm. The fabrication results of the other two sets of TSV structures with pure PETEOS oxide liner and pure low-*k* liner are reported previously in [11] and [12].



Element (atm %)	1	2	3	4
O		52.48	48.48	9.5
Al		1.87	38.62	
Si	0.48	41.51	10.66	88.23
Cl		0.13		
Cu	99.51	3.99	2.22	2.26

Fig. 2. FIB image of TSV and TEM close-up view of the liner stack.

Stress Modeling and Measurement

Finite element analysis in Fig.3 shows that low-*k* liner, with smaller elastic modulus (~7.2GPa), acts as a compliant layer to cushion the Cu-TSV stress on Si compared with PETEOS (75GPa). High resolution Raman spectroscopy is used to verify the biaxial stress exerted on Si. In Fig. 4(a), it is verified that with low-*k* liner, lower compressive stress is exerted by Cu-TSV on the Si between the TSV. This has

positive implication on variability, reliability and keep-out zone. The 2D stress map is presented in Fig. 4(b).

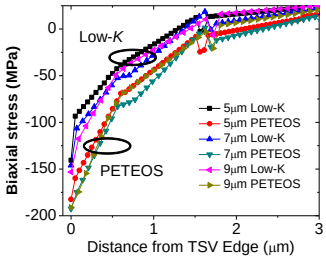


Fig. 3. (*FEA Simulation*) Thermo-mechanical stress exerted by a single Cu-TSV on Si as a function of distance from the edge of TSV.

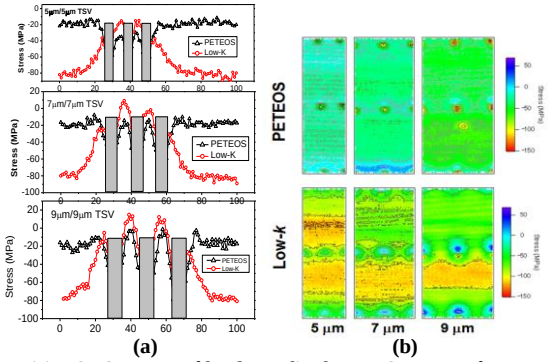


Fig. 4. (a) Si Stress profile (biaxial) along TSV rows from Raman Measurement (λ = 488 nm). Each row contains 3 TSV with similar TSV pitch and diameter (5, 7, 9 μm). The stress profiles show that low-κ liner is more compliant and can cushion stress exerted by Cu-TSV on the Si (between TSV) more effectively than PETEOS oxide; **(b)** Biaxial stress mapping of the Si based on micro-Raman spectroscopy.

Electrical Measurement Results

The measured *CV* curves at 100 kHz on TSV structures with PETEOS oxide liner, low-*k* liner and Al_2O_3/low-*k* bi-layer liner after annealing in forming gas (N_2/H_2) at 350 ℃ for 30min are shown in the Fig. 5(a). It is shown that by replacing the PETEOS oxide liner with the low-*k* liner which has an estimated dielectric constant of ~2.8, the accumulation capacitance is reduced by ~26%. As discussed in [11] and [13], fixed charge (Q_f) can effectively shift the V_{FB}. Due to the insertion of ~10 nm thin Al_2O_3 layer between Si and the low-*k* liner, a large amount of negative fixed charge is induced at the liner/Si interface and the charge density is on the order of ~ -1.3×10^{12} cm^{-2}. The negative fixed charge causes a positive shift in V_{FB} (ΔV_{FB} = +19V). As a result, TSV is operated in the stable accumulation capacitance region within the voltage of interests (~ 0-5 V) to overcome the spatial performance variation caused by non-uniform hotspot heating.

The effect of annealing on Al_2O_3/low-*k* liner is presented in Fig. 5(b) and the *k* value remains constant. With the insertion of Al_2O_3, the TSV is operated in the stable accumulation region between 0-5V and does not fluctuate with temperature (25 to 100°C) as shown in Fig. 5(c). Similar to [13], the stability of Al_2O_3-induced negative fix charge is also studied under prolonged biasing with a high electric field of 2 MV/cm. The result in Fig. 5(d) confirms that sufficient negative fixed charge is maintained even under electric field biasing.

IV measurement is performed and Fig. 6 presents the leakage current density of Al_2O_3/low-*k* bi-layer liner at an electric field of 2 MV/cm after annealing at various conditions. The result shows that annealing in forming gas at 350 ℃ for 2 hours or at 400 ℃ for 0.5 hour can significantly improve the leakage current and effectively reduce the leakage current density to a level of ~ 4×10^{-6} A/cm^2 at mid-distribution, comparable with that of PETEOS liner.

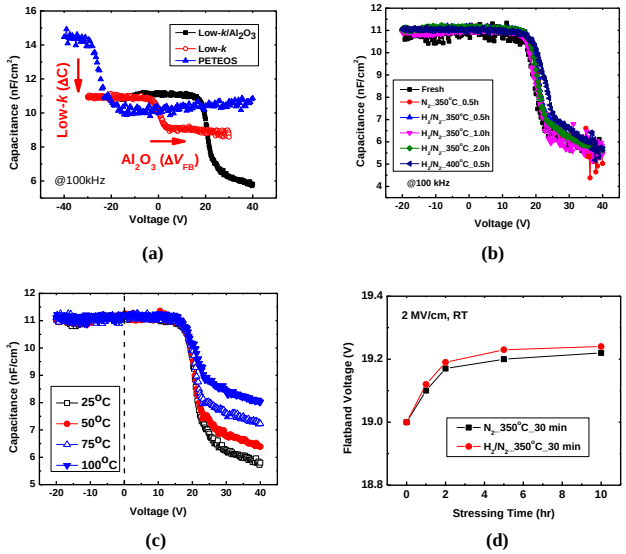


Fig. 5. (a) *CV* characteristics of TSV structures with different liners after annealing in forming gas (N_2/H_2) at 350 ℃ for 30min; **(b)** *CV* characteristics of TSV with Al_2O_3/low-κ liner after annealing at various conditions; **(c)** Stable accumulation capacitance within operating voltage of interest (0-5V) is achieved; **(d)** The stability of the negative fixed charge under 2 MV/cm biasing. The V_{FB} increases initially and stabilizes after 5 hours.

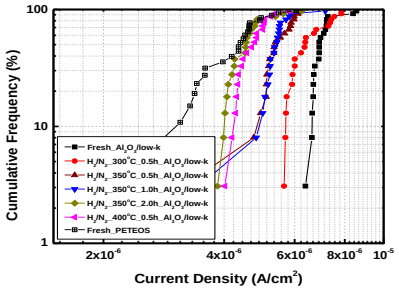


Fig. 6. *IV* measurement of Al_2O_3/low-κ bi-layer liner after annealing. Leakage current density is improved to a level comparable with PETEOS oxide liner after annealing in forming gas (N_2/H_2) at 350 ℃ for 2 hours or at 400 ℃ for 0.5 hour.

4. Conclusion

A novel material integration of thin Al_2O_3 with low-*k* bi-layer in the TSV structure as the liner has been successfully achieved and used to reduce TSV stress and a ~26% reduction in capacitance is obtained. Negative fixed charge induced in the thin Al_2O_3 layer causes positive flat-band voltage shift. TSV is operated in the stable accumulation region hence immune to spatial temperature variation.

References

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