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Analysis and reduction of leakage current of 2kV monolithic isolator with wide trench spiral isolation structure

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Abstract:
In this work, the origin of the leakage current of highly area efficient silicon-on-insulator (SOI) monolithic isolator using spiral trench isolation structure is clarified by experimental and simulation analyses and the its reduction method is proposed. It was found that parasitic MOSFET inversion and accumulation channels induced at the SOI and buried oxide (BOX) interface are the origins of leakage current. To reduce the leakage current, adequate thickness conditions of BOX layer are proposed for various voltage usage.

1. Introduction

The insulation devices are used for many devices as important parts of the Machine to Machine (M2M) systems interface. Small size, low cost with high reliability and safety are strongly required for such isolators. On-chip isolation structure is a promising technology. Recently, a detailed analysis results of breakdown voltage for SOI isolators using multi-trench gaps were reported[1-4]. This kind of structure shown in Fig.1 is considered to be suitable for monolithic isolators with no additional special processes. It has been clarified that the impedance of the insulation region between the separated two regions is crucial to the breakdown voltage, and among the various trench gap structures shown in Fig.2, the spiral type exhibited the highest figure-of-merit between the breakdown voltage and the leakage current for a given area[4]. However, the leakage current value is somewhat higher than that estimated by the simple series resistance of SOI spiral regions as it will be explained in the next section. In this work, the origin of the leakage current of spiral type isolator is clarified by experimental and simulation analyses and its reduction method is proposed.

2. Measured Leakage Current of Spiral Type

Figure 3 shows the measured current-voltage characteristics of a fabricated spiral type isolator. The center part was electrically connected to the Si substrate as shown in the figure. Here, the resistance between region 1 and region 2 was designed to be 500MΩ based on the resistivity of SOI layer (10 Ωcm) so that the leakage current becomes 4μA at 2kV usage. However, the obtained actual leakage current quadratically increased as an increase of applied voltage, and it reached 80μA at 2kV, which is 20-times larger than the estimation. The origin of this deviation is to be analyzed in the next section.

3. Analysis and Reduction Method of Leakage Current

Figure 4 shows the schematic illustration of the carrier distribution in the spiral type isolation based on the device simulation result. It was clarified that at the SOI-BOX-Substrate, a charge distribution follows the device physics of MOS capacitor system with Si substrate as the gate electrode. Thus, when the SOI voltage is lower than that of substrate, electron inversion layer tends to be generated at SOI/BOX interface. Likewise when the SOI voltage is higher than that of substrate, hole accumulation layer is generated. Therefore, for the spiral type isolator, rather than a simple series resistance model, the series connection model of the inversion-mode and the accumulation-mode MOSFETs[6] should be taken into account as shown in Fig.5. Then, the leakage current behavior was calculated based on the proposed model. The formula used for the calculation is summarized in Fig.6. The obtained result is shown in Fig.7 with the measurement result of the fabricated sample. As shown in the figure, the calculated result agrees well with the measurement result, indicating that using the proposed model we can estimate the leakage current values for various structures. Using the same calculation method, the effective resistance values were obtained for various BOX thickness for 500V to 2kV usage as shown in Fig.8. As shown in the figure, the effective resistance increases as BOX thickness increases because Cox is decreased and the carrier concentrations at inversion and accumulation layers become lower. Based on the obtained result, suitable BOX thickness conditions were proposed for specific voltage usage, such that, BOX thickness should be 65μm or more for obtaining 500MΩ at 2kV, and it should be 15μm or more for 500MΩ at 500V. SOI wafer with thermal oxidation can be used for BOX in less than 20μm thickness. For more than 20μm BOX thickness, ceramics or glass substrate can be used.

4. Conclusions

The origin and behavior of the leakage current in the SOI monolithic insulator using spiral trench isolation structure was analyzed and it was found that the MOSFET inversion and accumulation channels at SOI/BOX interface are the origins. Using the developed series MOSFETs model, adequate BOX thickness conditions were obtained for various voltage specs. The developed model is useful for the design of small area, low and highly reliable cost monolithic isolators.

References

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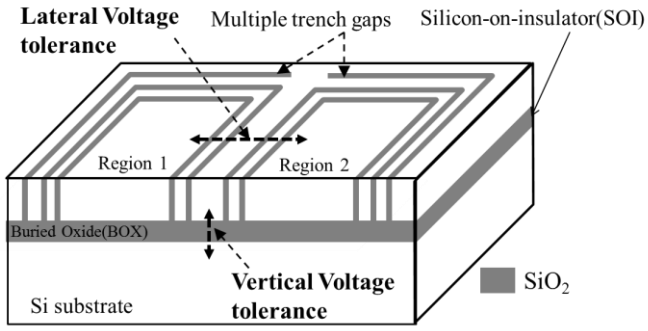

Figure1. Schematic chip view of multiple trench isolation [1)–4)].

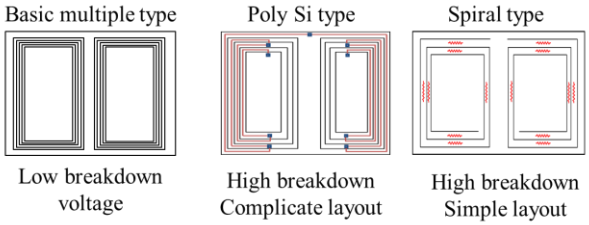

Figure 2. Multiple trench isolation layouts.

Parameters	Value
Buried oxide thickness	3.0μm
SOI thickness	1.5μ m
Trench width	10μ m
SOI length between region1 and region 2	37.8 mm
SOI width	5 μm
SOI resistivity	10 Ωcm
SOI type	P type

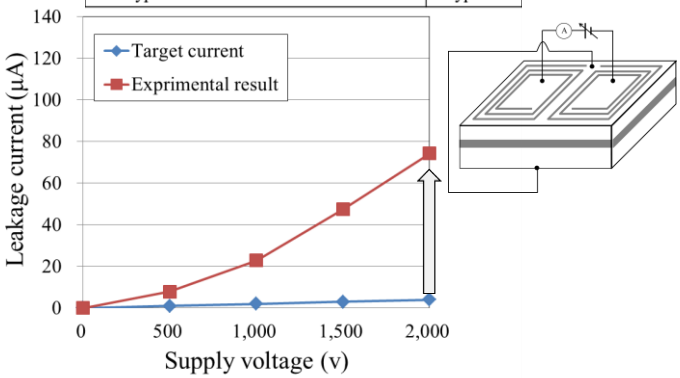

Figure 3.Experimental result of Leakage current of spiral type isolation device. Target current only take into account the resistivity of SOI.

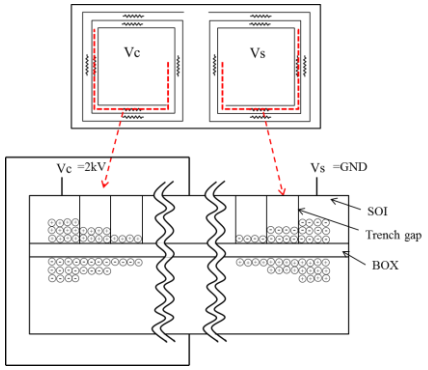

Figure 4. Carrier distribution in spiral type isolation structure.

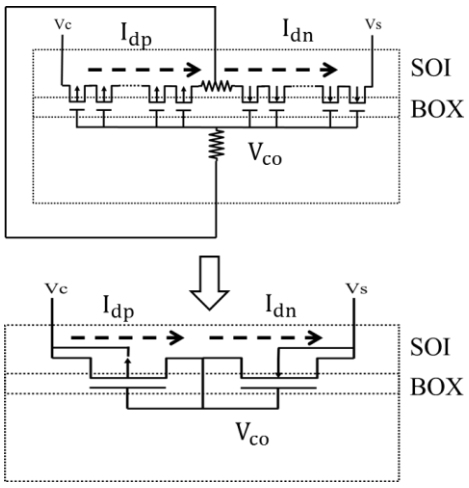

Figure 5. Simplified electrical model of spiral type isolation structure.

$$I_{dn} = \frac{1}{2}\frac{W}{L}\mu_n C_{ox}\left[2(V_{co}-V_{tn})V_{co}-V_{co}^2\right] \quad (1)$$

$$I_{dp} = \frac{1}{2}\frac{W}{L}\mu_p C_{ox}\left[2(V_c-V_{co}-V_{tp})(V_c-V_{co})-(V_c-V_{co})^2\right] \quad (2)$$

$$V_{co} = \frac{\left(\frac{\mu_n}{\mu_p}V_{tn}+V_{tp}-V_c\right)+\sqrt{\left(\frac{\mu_n}{\mu_p}V_{tn}+V_{tp}-V_c\right)^2-\left(\frac{\mu_n}{\mu_p}-1\right)(2V_{tp}-V_c)V_c}}{\left(\frac{\mu_n}{\mu_p}-1\right)} \quad (3)$$

Figure 6. Formula used for the analysis of leakage current.

Parameters	Value
Electron mobility	900 cm²/Vs
Hole mobility	400 cm²/Vs
n type threshold voltage	30V
P type threshold voltage	-30V

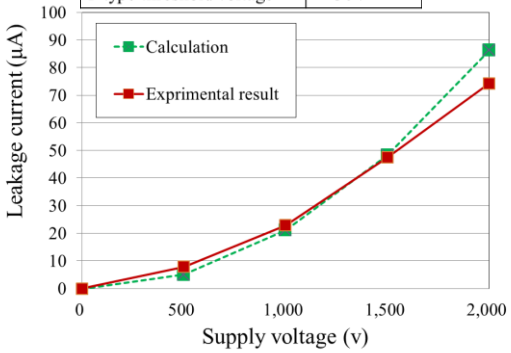

Figure 7. Analytical result of spiral isolation device.

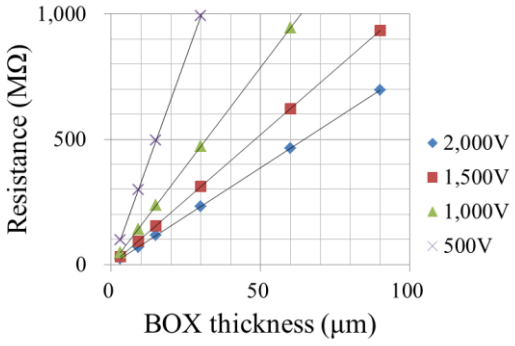

Figure 8. Effective resistance of spiral isolation device as a function of BOX thickness.