

VLSI Pulse-Coupled Phase Oscillator Networks and Their Emulator toward Spike-based Computation for Intelligent Processing

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Abstract

Spike-based computation plays a key role in constructing brain-like intelligent systems. It is a time-domain computation in which information is encoded by the timing of spike pulses. A pulse-coupled phase oscillator can be described using spike-based computation. In our previous study, we proposed VLSI pulse-coupled phase oscillator networks and their corresponding FPGA emulators. In this paper, we demonstrate image region segmentation by using the proposed digital VLSI emulator implemented in an FPGA and show the effectiveness of spike-based computation in terms of large-scale integration.

1. Introduction

Neurons communicate by spike pulses, with the network of neurons (i.e. neural networks) performing intelligent information processing in the brain. Brain-like intelligent systems attempt to mimic this brain architecture. Here, spike-based computation is essential function to implement a physical artificial intelligence and it is a promising way to realize *more than Moore* large-scale integration.

To implement spike-based computation and show its effectiveness, in our previous study, we focused on pulse-coupled phase oscillator systems and proposed a corresponding very-large-scale integration (VLSI) architecture [1]. We also proposed a field-programmable gate array (FPGA) emulator of pulse-coupled phase oscillator systems to simulate a variety of networks with complicated interconnections [2].

Compared with fully digital systems, spike-based computation has advantages in terms of power consumption and wiring area from the view point of large-scale integration. In this paper, we review the architecture of pulse-coupled phase oscillator networks, then demonstrate image region segmentation by using the proposed digital VLSI emulator implemented in an FPGA.

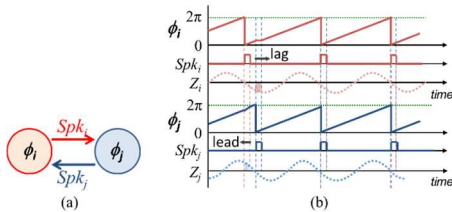


Fig. 1 Dynamics of pulse-coupled phase oscillators: (a) network schematic of two oscillators, and (b) its dynamics.

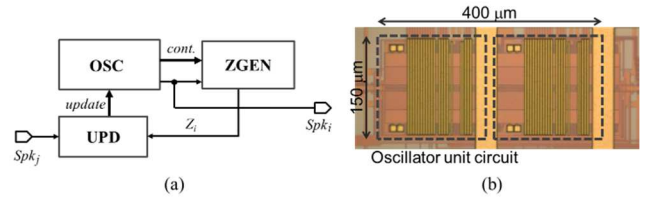


Fig. 2 Pulse-coupled phase oscillator circuit: (a) block diagram, and (b) microphotograph of two pulse-coupled oscillator circuits.

2. Pulse-coupled phase oscillator model

The concept of coupled phase oscillators was first proposed by Winfree [3]. For digital hardware implementation, we proposed a discretized model and its dynamics expressed as follows [2]:

$$\phi_i(t+1) = \phi_i(t) + \omega_i + Z(\phi_i) \frac{K_0}{N} \sum_{j=1}^N Spk_j(t) \quad (1)$$

$$Spk_j(t) = \begin{cases} 1 & \phi_j(t) = \phi_{th} \\ 0 & \text{otherwise} \end{cases} \quad (2)$$

where ϕ_i is the i -th phase variable with 2π periodicity, ω_i is the i -th natural angular frequency, $Z(\phi_i)$ is a phase sensitivity function that outputs the response of the i -th oscillator, K_0 is the coupling strength, N is the number of oscillators, and $Spk_j(t)$ is the input from the j -th oscillator. The oscillator outputs a spike pulse when the phase variable reaches threshold value ϕ_{th} , then resets its value as $\phi_i = 0$.

Figure 1 shows the dynamics of pulse-coupled oscillators. We assume the phase sensitivity function is $Z(\phi_i) = -\sin(\phi_i)$. In this case, two oscillators are coupled with spike pulses Spk_i and Spk_j as shown in Fig. 1 (a). Phase variables ϕ_i and ϕ_j are updated by spike pulse inputs from the coupled oscillator, with the updated value calculated by a response of function $Z(\phi)$ as shown in Fig. 1(b).

For oscillator i , the response from oscillator j is obtained by referencing $Z(\phi_i)$ when Spk_j is fed into oscillator i , i.e., a physical connection between oscillators needs only one bit per oscillator for spike pulse communication. This feature is therefore suitable for hardware implementation within a large-scale network and is the most important advantage of using this model.

3. VLSI pulse-coupled phase oscillator networks and FPGA emulator

We proposed analog VLSI pulse-coupled phase os-

cillator networks [1]. Figure 2(a) shows a simplified block diagram of the proposed oscillator circuit consisting of oscillator OSC, phase sensitivity function generator ZGEN, and phase state updater UPD. A microphotograph of two pulse-coupled oscillator unit circuits is shown in Fig. 2(b). Illustrated in Fig. 2(a), oscillators are coupled by one-bit spike pulses Spk_i and Spk_j . This architecture therefore can be implemented with a low wiring area and fits well with large-scale integration in a massively parallel manner.

In our analog VLSI implementation, OSC stores phase variable ϕ_i , and generates spike pulses Spk_i . Phase variable ϕ_i is represented by charges stored at a capacitor, which is charged with current sources for summing current value $\phi_i(t)$ and natural angular frequency ω_i . The ZGEN generates the shape of phase sensitivity function $Z(\phi_i)$ using control signals from OSC. The UPD then determines the update value by referencing function $Z(\phi_i)$ when Spk_j is fed into the oscillator unit circuit.

Although the analog VLSI implementation is appropriate for realizing brain-like systems with very low-power consumption, it is disadvantageous in terms of its reconfigurability to changes in network size and interconnections. It also inevitably suffers from device parameter mismatch and variability.

Therefore, we proposed a parameterized digital design for pulse-coupled phase oscillator networks [2]. In this design, OSC is represented by a configurable counter circuit and ZGEN and UPD are constructed by combination circuits. The proposed design is described by parameterized Verilog HDL and executed on an FPGA. This FPGA implementation can realize a variety of networks by changing the given parameters.

4. Experimental results of image region segmentation

Region-based coupled Markov random field (MRF) is a computational model that explains the visual cortex in the brain [4]. It provides practical image processing, including image region segmentation, and can be represented by a combination of pulse-coupled phase oscillators.

We proposed an efficient pixel-parallel image processing method using the pulse-coupled phase oscillator model and its analog VLSI implementation, as shown in Fig. 3(a) [5]. Two oscillators that correspond to intensity and label processes are assigned to a pixel, and a grid consisting of up to 30×30 pixels can be processed, as shown in Figs. 3(b) and (c). The performance power-consumption ratio of 656 GOPS/W is very high in comparison with existing digital processors. Thus, results show that spike-based computation is effective for realizing brain-like systems with very low-power consumption; however, the analog VLSI implementation has problems with calculation accuracy and fluctuations due to device mismatches, as shown in Fig. 3(d).

To solve these problems, we developed an FPGA emulator to realize the MRF model. Results of emulation and a specification of the FPGA emulator are shown in Figs. 4(a) and (b), respectively. Results show clear region segmenta-

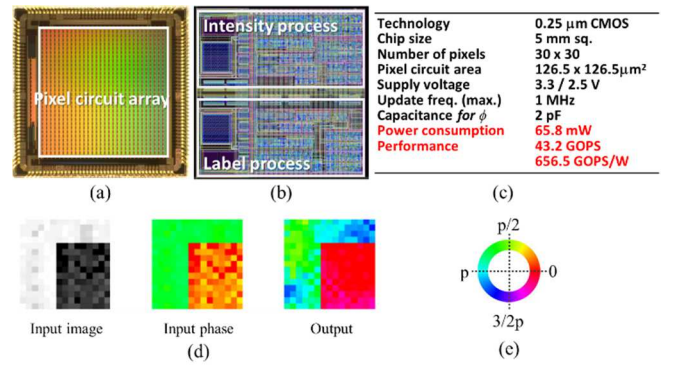


Fig. 3 Analog VLSI implementation of MRF model: (a) chip micrograph, (b) pixel circuit based on two oscillators, (c) chip specification, (d) results of image segmentation, and (e) color chart of phase variable.

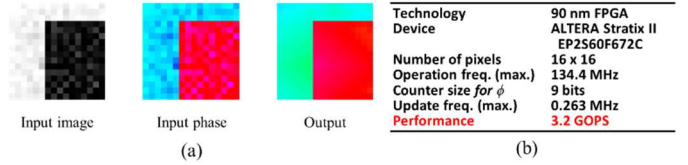


Fig. 4 Results of FPGA emulator: (a) results of image segmentation, and (b) specification.

tion because the FPGA emulator performed accurate calculation based on digital processing. Therefore, it is useful for finding problems in VLSI design and exploring new applications or architectures based on spike-based computation.

5. Conclusions

Spike-based computation is a promising approach to realizing brain-like intelligent systems. The proposed analog VLSI implementation of pulse-coupled phase oscillator networks achieved very low-power consumption processing for image region segmentation. Further, the FPGA implementation emulated various network structures.

To implement the pulse-coupled phase oscillators, three functions are essential, i.e., oscillation, the generation of phase sensitive functions, and the proper updating of phase variables. If we can implement these functions using nanodevices, we will drastically reduce power consumption and circuit footprints of pulse-coupled phase oscillators. To achieve this, it is crucial for circuit designers to collaborate with device and material researchers.

Acknowledgements

This work was partly supported by JSPS KAKENHI Grant Numbers 15H01706 and 15K12110.

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