Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp808-809

Reconfigurable Hybrid Parallel Vision Processor with Full-custom Compact Distributed Memory

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Abstract

This paper presents the reconfigurable hybrid parallel vision processor based on the compact distributed memory. The processor consists of a processing element (PE) array with the compact distributed memory, a row processor (RP) array, a dual-core microprocessor and a neural network. We propose an enhanced memory architecture with compact area and design the memory in a full-custom way to save chip area. The vision processor has been fabricated in a 0.18 μm 1P5M CMOS technology. The area of the memory is reduced remarkably and is less than 1/3 of the memory based on the conventional cell structure. The vision processor area has been reduced by 44%. The chip experimental results demonstrate that the presented chip achieves correct image processing functions.

1. Introduction

The vision chip integrates the image sensor and the vision processor on a single chip to achieve high processing speed and low power consumption [1]. The PE array is one of the critical components in the vision chip [2] and can be reconfigured into a self-organizing map (SOM) neural network that performs the high level image processing [3]. The PE array consists of the arithmetic-logic units (ALUs) and the distributed memory. The memory occupies most of the circuit area of the PE array and it limits the scale of the PE array. This paper proposes an enhanced memory architecture with compact area and designs the memory in a full-custom way to save chip area and implements a reconfigurable hybrid parallel vision processor based on the proposed memory. The area of the memory is reduced remarkably and is less than 1/3 of the memory based on the conventional cell structure while the overall chip area has been reduced by 44%. Preliminary test results demonstrate that the presented vision processor achieves correct functions.

2. Vision processor architecture

The vision processor inherits the hybrid parallel architecture from our previous work [3]. Fig. 1 illustrates the architecture of the vision processor. The processor consists of a 64 × 64 PE array, a 64 row processor (RP) array, a dual-core RISC processor and a 16 × 16 SOM neural network. The PE array and the SOM neural network can be dynamically reconfigured from each other. Each PE consists of a 1-bit ALU and a distributed memory: 64-bit RAM. The ALU loads (writes) data from (to) the RAM and four adjacent PEs, and can perform 1-bit AND, OR, NOT and ADD operations. Decoded operating and addressing signals control the processor in a single instruction multiple data (SIMD) fashion.

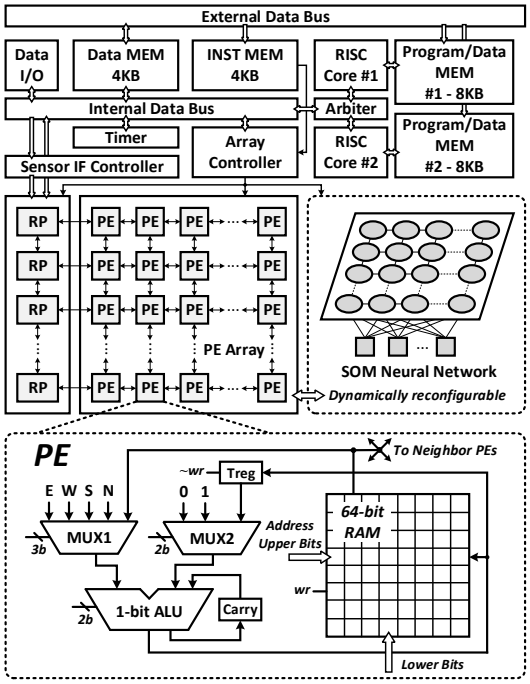

Fig. 1 Architecture of the vision processor.

3. Implementation and fabrication

Full-custom 64-bit RAM

Fig. 2 shows the proposed architecture of the 64-bit RAM. The RAM consists of 8 rows of two-stage registers. Each row contains 8 7-transistor (7-T) SLs as the master stage and a 4-transistor (4-T) dynamic latch (DL) as the slave stage. The transmission gate in the SL forms a feedback loop to keep the stored signal. The weak PMOS transistor in the DL forms another feedback path to recover the high signal level and reduce the static power consumption. The automatically refreshment of the DL helps retain the signal state in the slave stage. Compared with conventional RAM cell, the proposed RAM uses less transistors with the smallest feature size so the memory area is compact. Fig. 3 shows partial layout of the 0.18 μm-process RAM with the size of 30.7 μm ×7.7μm.

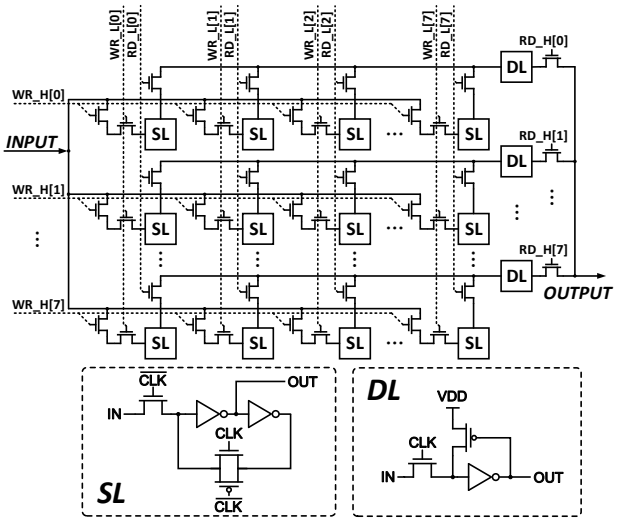

Fig. 2 Architecture of the distributed memory.

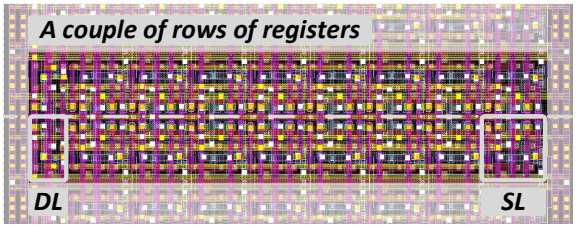

Fig. 3 Layout of the compact distributed memory.

Balanced clock tree design

In order to achieve the synchronization between the processing circuits and the manually designed memory, we designed a two-layer balanced clock tree. The 1st layer of the clock tree is formed by a common inverter driving the input clock to the 16 × 16 SOM neural network. The 2nd layer of the clock tree is designed inside each neuron by evaluating the load capacitance of each clock input node in the 16 × 16 PE array, as Fig. 4 shows. The compact clock tree can make the ALUs and the distributed memory in the PE array operate synchronously.

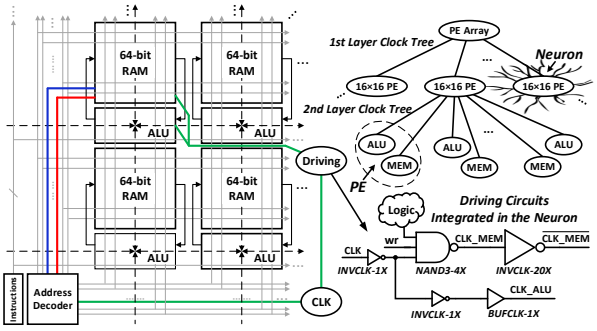

Fig. 4 Implementation of the balanced clock tree.

Fig.5 shows the microphotograph of the chip fabricated in a 0.18 μm 1P5M CMOS technology. The core area is 4.58 × 4.27 mm^2. Compared with [3] designed in conventional design flow, the vision processor achieves 44% area saving while reserving the same processing architecture.

Fig. 5 Microphotograph of the fabricated chip.

4. Experimental results

The test platform shown in Fig. 6 is equipped with the chip, a QVGA image sensor and a FPGA. Preliminary test results show that image processing operations can be fulfilled in high speed. Fig. 7(a) shows the image processing results and Fig. 7(b) shows the area measurement result of the architecture presented in this paper.

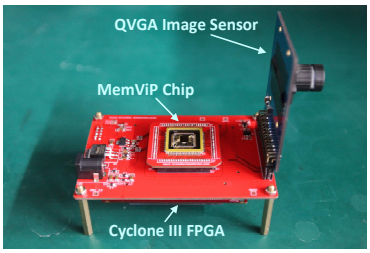

Fig. 6 Test platform for the vision processor.

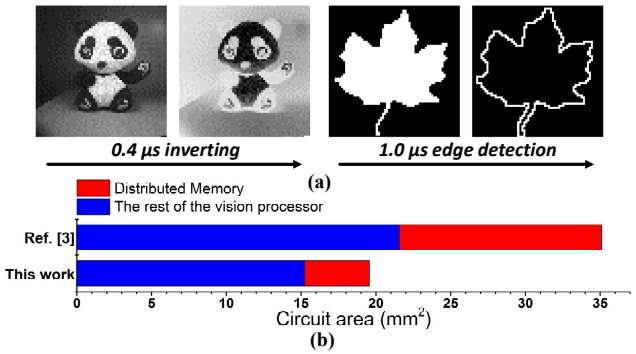

Fig. 7 (a) Image processing results. (b) Area measurement result.

5. Conclusions

A reconfigurable hybrid parallel vision processor with full-custom distributed memory has been proposed in this paper. The area of the memory has been remarkably reduced by optimizing the design in both of the transistor level and the physical level. The vision processor area has been reduced by 44% while the image processing function is well reserved.

References

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