

Low Contrast Motion Capturing Vision Sensor with Crystalline Oxide Semiconductor FET-based In-Pixel Threshold Voltage Compensation Circuit

S. Maeda¹, T. Ohmaru¹, H. Inoue¹, T. Nakagawa¹, Y. Kurokawa¹, T. Ikeda¹,
Y. Suzuki¹, N. Yamade¹, H. Miyairi¹, M. Ikeda², and S. Yamazaki¹

¹Semiconductor Energy Laboratory Co., Ltd., 398 Hase, Atsugi, Kanagawa, 243-0036, Japan
Phone: +81-46-248-1131 E-mail: sm1179@sel.co.jp

²The University of Tokyo, 2-11-16 Yayoi, Bunkyo-ku, Tokyo, 113-0032, Japan

Abstract

To improve uniformity between pixels in a vision sensor with a motion capturing function, an in-pixel threshold voltage (V_{th}) compensation circuit employs c-axis aligned crystalline oxide semiconductor (CAAC-OS) FETs. The vision sensor shows that this configuration reduces fixed pattern noise of the vision sensor by 16.2% and offers a 2.05-fold improvement in motion-capturing sensitivity.

1. Introduction

Utilizing the extremely low off-state current of crystalline oxide semiconductor FETs, mainly c-axis aligned crystalline oxide semiconductor (CAAC-OS) FETs[1], an electronic global shutter image sensor was proposed[2,3]. A motion capturing vision sensor that has nonvolatile analog memory comprising a CAAC-OS FET in each pixel was also proposed[4]. The vision sensor achieves motion capturing by storing captured data of a reference frame in the nonvolatile analog memory in the pixel and calculating a difference between the reference frame and the current frame in the pixel, then judging the difference in a motion detector based on a reference level. To detect a slight difference in low contrast, a range of the reference level in a motion detector should be narrow. Therefore, motion capturing-sensitivity highly depends on pixel uniformity. Complete correlated double sampling (CDS) is not available for the vision sensor with motion capturing function because it stores the data in a reference frame in the pixel.

In this study, the motion capturing vision sensor is redesigned to improve motion capturing-sensitivity by employing a circuit for compensating the threshold voltage (V_{th}) of an amplifier transistor in each pixel.

2. Circuit Design

The vision sensor consists of a pixel array, a row driver, a column driver, an A/D converter and a motion detector. The motion detector and an A/D converter operate exclusively; therefore, the vision sensor can perform both motion capturing and normal capturing.

The configuration of a pixel circuit with a V_{th} compensation circuit in the vision sensor and its operation timing diagram are shown in Fig. 1. In the pixel circuit, the V_{th} compensation circuit is achieved by adding two transistors and two capacitors to the pixel circuit of the motion capturing vision sensor fabricated in [4]. The V_{th} compensation of the pixel circuit is described as follows. First in T1a, the voltage of the capacitor C4 is initialized by

setting VPO at V_{POH} and BR at V_{BRH} . In T2a, the voltage of the node AG is discharged until it reaches to $(V_{POH} + V_{th_M4})$, where V_{th_M4} is the threshold voltage of the transistor M4. Here, V_{POH} is the pixel output when there is no differential data in the pixel, i.e., the reference output level. In this case, the voltage of the node FD (V_{FD}) and the voltage of the node AG (V_{AG}) are set at initial voltage V_{FD0} and V_{AG0} , respectively. In T3a, AG is set in a floating state and V_{th_M4} is retained in the capacitor C4. Finally, in T4a, the V_{th} compensation is completed.

In the case where the transistor M4 is used as a source follower circuit, pixel output voltage equals $(V_{AG} - V_{th})$. Here, V_{AG} equals $\{V_{AG0} + \alpha(V_{FD} - V_{FD0})\}$, where α is a coupling coefficient. Therefore, the pixel output voltage equals $\{V_{AG0} - V_{th_M4} + \alpha(V_{FD} - V_{FD0})\}$, or $\{V_{POH} + \alpha(V_{FD} - V_{FD0})\}$, which does not depend on V_{th_M4} . All the in-pixel transistors are CAAC-OS FETs; therefore, V_{th} data can be retained for a long time and the V_{th} compensation in each frame is not required.

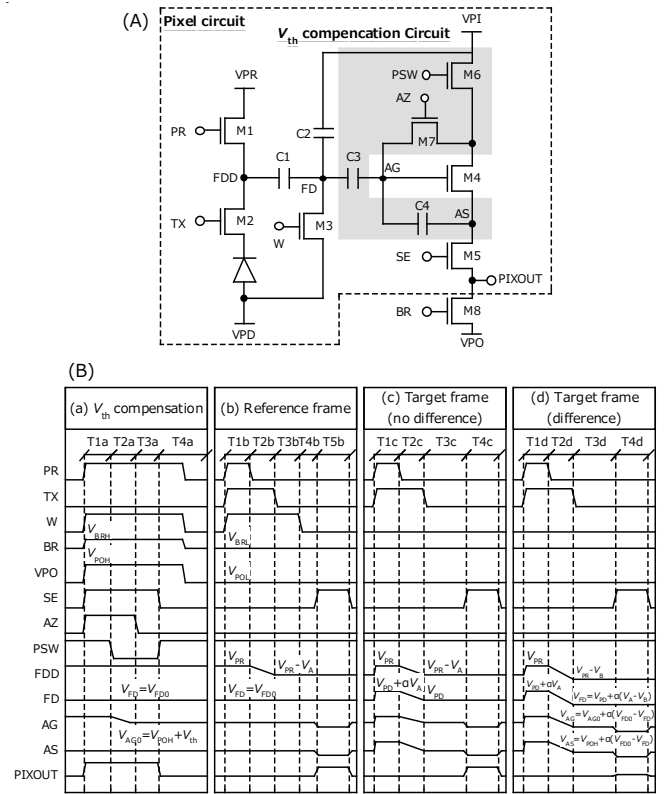


Fig. 1 V_{th} compensation pixel circuit (A) and operation timing (B).

Motion capturing operation[4] is described in Figs. 1B(b) to 1B(d). First, in the reference frame, during the exposure time (T2b), charge corresponding to the intensity of light is accumulated in the node FDD while V_{FD} is fixed to V_{FD0} . On the other hand, in the target frame, during the exposure time (T2c or T2d), FD is in a floating state. Accordingly, when data of the target frame are the same as the data of the reference frame, V_{FD} is returned to the initial voltage V_{FD0} after capturing, and the pixel output level is the same as the reference output level (T4c). In contrast, when the data of the target frame are different from the data of the reference frame, V_{FD} is changed from V_{FD0} depending on the differential data, and the pixel output level is different from the reference output level (T4d). The motion detector compares the pixel output level with the reference voltage ranging from V_{REF+} to V_{REF-} using comparators. When the pixel output level exceed the reference voltage, it outputs a 1-bit motion trigger.

3. Measurement Results

The vision sensors are fabricated with and without a V_{th} compensation circuit in the pixel by CAAC-OS FET/Si FET hybrid process. The specifications of the vision sensor are listed in Table I.

Fig. 2A shows the histogram of 8-bit A/D converted output values of all the pixels with various V_{FD} . The histograms indicate that the uniformity of pixel output of the vision sensor with the V_{th} compensation circuit is increased at each output value. The standard deviation between the pixels at each output value is calculated from Fig. 2A. The V_{th} compensation circuit reduces variation between the pixels by 1.39 at 120 of the output value, for example. Please note that it is confirmed that output gain variation of the vision sensor is increased by 37.8% compared with the vision sensor without the V_{th} compensation circuit due to the increase in the number of pixel transistors and capacitance variation, and that the output offset variation is reduced by 22.2%. Furthermore, FPN of the vision sensor with the V_{th} compensation circuit is confirmed to be reduced by 16.2%.

The motion capturing accuracies in the vision sensors with and without the V_{th} compensation circuits are compared. We measure the closest values of V_{REF+} and V_{REF-} at a certain reference output level in a condition where the motion detector does not output the motion trigger. Here, as $\Delta V_{REF} (= V_{REF+} - V_{REF-})$ becomes smaller, the motion detector can detect even a slight difference and can reduce detection errors, which means the higher sensitivity. Fig. 2B shows the results. At 120 of the output value, for example, the V_{th} compensation circuit reduces ΔV_{REF} from 200 mV to 97.5 mV. This offers a 2.05-fold improvement in capturing sensitivity.

Fig. 3 shows the motion capturing results when a target object of the reference frame is a blank sheet and a target object of the target frame is a character-printed sheet. Here, we show results of the experiments using sheets with printed characters "A" of different depths of colors as target objects. It is clear that the vision sensor with V_{th} compensation circuit can detect a slight difference due to improvement in capturing sensitivity.

Please note that the amount of variation between the pixels after one hour from V_{th} compensation is confirmed to be approximately 8%. That is, if V_{th} compensation is repeated very infrequently, for example, once every few hours, the V_{th} compensation effect can be maintained permanently. This is due to retention of the voltage of the capacitor using the extremely low off-state current of the CAAC-OS FET.

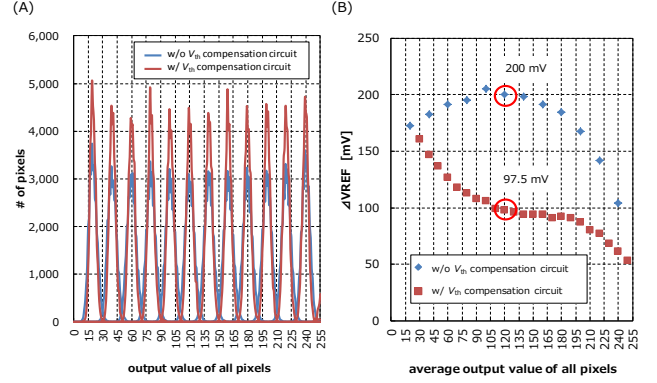


Fig. 2 Output distribution of all pixels (A) and motion capturing range ΔV_{REF} in average output value of all pixels (B).

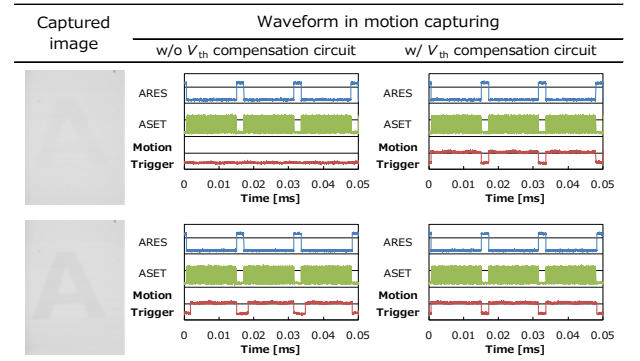


Fig. 3 Comparison of motion capturing with and without V_{th} compensation.

4. Conclusion

We have proposed in-pixel V_{th} compensation circuit for the vision sensor. This configuration reduces FPN of the vision sensor by 16.2% and offers a 2.05-fold improvement in motion-capturing sensitivity. Consequently, the vision sensor can capture the motion even when the object is changed slightly.

Table I Specifications of vision sensor.

	w/o V_{th} compensation circuit	w/ V_{th} compensation circuit
Process	0.5 μ m N-ch CAAC-OS	
technology	0.18 μ m P-ch Si	
Die Size	6.5 mm \times 6.5 mm	
Number of pixels	240 \times 160	
Pixel size	20 μ m \times 20 μ m	
Pixel configuration	5 transistors, 2 capacitors	7 transistors, 4 capacitors
Fill factor	29.75%	28.25%
FPN	1.73%	1.45%
Contrast sensitivity	200 mV	97.5 mV
	at 120 of the output value	at 120 of the output value
Power supply	I/O: 1.8 V	
	pixel, driver, ADC, analog: 3.3 V	
ADC	8-bit single slope	

References

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