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A CMOS SPAD Sensor Featuring Asynchronous Event-Extraction Readout Architecture for Faint Light Detection

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Abstract

Asynchronous event-extraction readout architecture is developed to reduce the computation and data transmission in single photon avalanche diode (SPAD) based faint light detection systems. By the measurement results from real fabricated chips, the functionality and efficiency of the architecture are experimentally demonstrated.

1. Introduction

Operating at Geiger mode, single photon avalanche diodes (SPADs) have such an ultra-high sensitivity that even faint light can cause immediate breakdown events. The high sensitivity of SPAD is mainly utilized for two purposes: the flight time detection and the faint light detection. The former includes 3D depth sensors and fluorescence lifetime imaging systems; while the latter includes positron emission tomography (PET) [1]. Different from ordinary photodiodes which output analog (gray scale) data, the output of a SPAD is digital since the SPAD can only be in two meaningful statues: the stable and the breakdown. One merit of the digital output over its analog counterpart is the robustness that significantly broadens the trade-off capability in the design of readout architecture. Namely, more aggressive architecture can be employed to achieve high functionality and efficiency.

In the particular case of faint light detection such as PET, the breakdown SPAD pixels are usually very sparse [2]. However, in the traditional readout architecture, the entire frame is firstly read out indifferent with the low number of events, and then processed to identify the locations of events, which are used for tomography. Because there are usually thousands of SPAD sensors operating simultaneously in a PET system [3], it can reduce a lot of computation and data transmission if the locations of events are extracted on the sensor. As a result, event-extraction readout architecture for SPAD sensors is highly demanded in such systems.

In this work, event-extraction readout architecture is developed for SPAD sensors. Asynchronous circuit technique is employed to parallel search all rows of the SPAD pixel array with the majority stable (non-breakdown) pixels skipped automatically. When a breakdown pixel is captured in the search, the column address of the pixel is readout by the output chain of the row. The location of the event is extracted by combining the column address with the address of the corresponding row. A test-of-concept chip with a 15×15 SPAD pixel array was developed using a standard 0.18 μm 5-Metal CMOS process. By measurement results, the functionality and efficiency of the proposed architecture are experimentally demonstrated.

2. Sensor Architecture

Idea of Asynchronous Event-Extraction Readout

Fig. 1 illustrates the procedure of the asynchronous event-extraction readout of one row. The process is triggered by activating the leftmost search signal (the red line in Fig. 1(a)). The activation begins to propagate along the search chain, activating each search signal of the stable pixel it passes asynchronously until it is blocked by an event pixel (Fig. 1(b)). Then, a global readout_en/search_continue (RE_SC) pulse signal is broadcast to resume the activation propagation and to connect the column address of the event pixel to the row's output chain for readout (Fig. 1(c)). Such an event capture and readout process is repeated (Fig. 1(d)) until the rightmost search signal is activated, which ends the event extraction of this row (Fig. 1(e)).

Chip Architecture

Fig. 2(a) shows the overall architecture of the chip which contains a 15x15 SPAD pixel array, a column address generator, and a global search finish detection block. Each pixel contains a SPAD [4], a quenching and breakdown capturing circuit (QBCC), and a column address readout circuit (CARC) as shown in Fig. 2(b). Fig. 2(c) shows the design of QBCC with the SPAD. If the SPAD is breakdown, the output signal "QC_OUT" is high. The signal "QC_EN" is used to control the window time of the SPAD sensor.

Asynchronous Event-Extraction Readout Architecture

Fig. 3(a) shows the inputs and outputs of the CARC in each pixel and the interconnections between neighboring CARCs. "Search[i-1]" and "Search[i]" are signals along the search chain. "Address[i]" is broadcast to all rows by the column address generator. The "Address_out" signals of all pixels in this row are connected together as the output chain.

Fig. 3(b) shows the design of CARC. After initialization, "Mask[i]" is low so that "$\overline{\text{QC\_OUT[i]}}$" is connected to the gate of M0. There are two cases when "Search[i-1]" is triggered, one is the case that "QC_OUT[i]" is low (the SPAD is stable), the other is the case that value of "QC_OUT[i]" is high (the SPAD is breakdown). In the former situation, M0 keeps on. When "Search[i-1]" goes high, the high voltage propagates to "Search[i]" after a delay of two gates.

In the other situation, M0 is off at the beginning. When "Search[i-1]" goes high, the lower input of the AND gate keeps high and "Search[i]" keeps low. In this way, the search signal is temporarily blocked at this pixel. When the global

"RE_SC" pulse signal goes high, "Mask[i]" goes high so that the column address can be readout and M0 becomes on. Therefore, the activation propagates to "Search[i]". At the same time, "address[i]" is readout since both M1 and M2 are on. When "RE_SC" is triggered to high again, the value of "Mask[i]" returns low, and "Address _out" is connected to the next breakdown pixel if such a pixel exists.

3. Experimental Results

The SPAD sensor was fabricated in a 0.18 μm standard 1P5M CMOS process. Fig. 4(a) shows a photomicrograph of the chip with the specification in Fig. 4(b).

Fig. 5 shows the measurement results when a chip was tested by a logic analyzer (Agilent 16822A). "Search[0]" (Fig. 5(b)), "RE_SC", and readout control signal (Fig. 5(a)) are inputs. Fig. 5(c) shows the measured "Address_out" indicating that the 9th and 13th pixels of this row are breakdown. The search finish signal goes high after all the pixels had been searched (Fig. 5(b)).

Fig. 6(a) is taken under dark condition, and the sum of 100 consecutive frames taken in the same condition are shown in Fig. 6(b). Fig. 6(c) is taken under light condition.

4. Conclusions

Event-extraction readout architecture employing asynchronous circuit technique is proposed. The functionality and efficiency of this architecture are experimentally demonstrated by the fabricated chip.

Acknowledgements

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References

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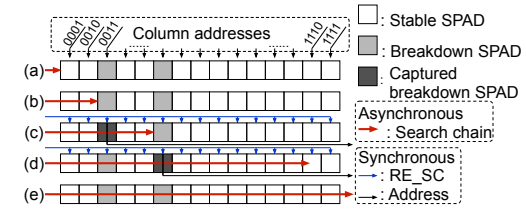


Fig. 1 Procedure of asynchronous event-extraction.

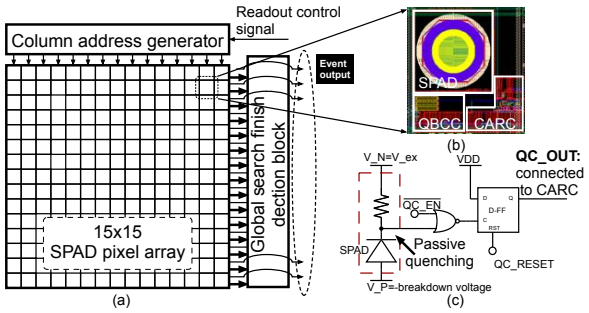


Fig. 2 (a) Chip architecture; (b) pixel layout; (c) design of QBCC.

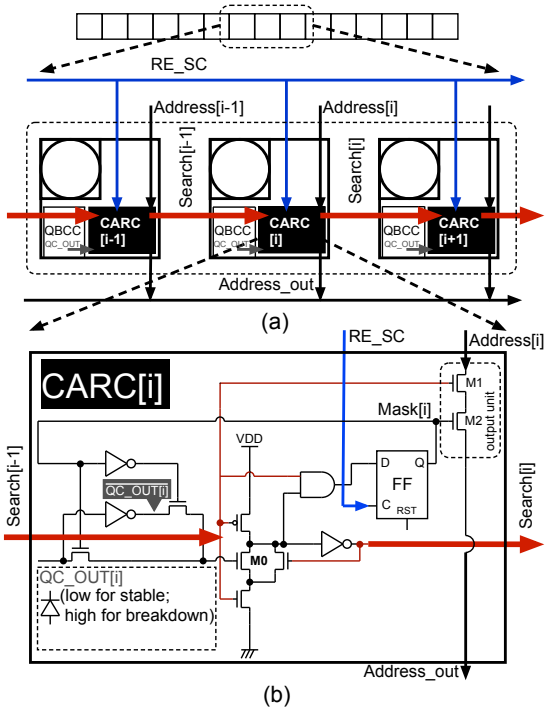
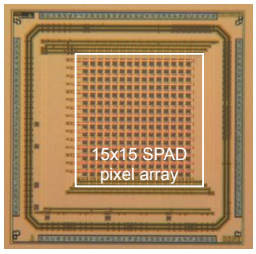


Fig. 3 Design of CARC: (a) interconnection between pixels; (b) detailed circuits of CARC.



Sensor characteristics	
Technology	0.18 μm 1P5M CMOS
Array size	15 x 15
Pixel size	80 μm x 80 μm
Fill factor	6.25%
Sensor core size	1.68 mm x1.68 mm
SPAD characteristics	
Breakdown Voltage	27V
Dark Count Rate	20.2kHz@Vex=1.8V

(b)

Fig. 4 (a) Photomicrograph of the chip; (b) specification.

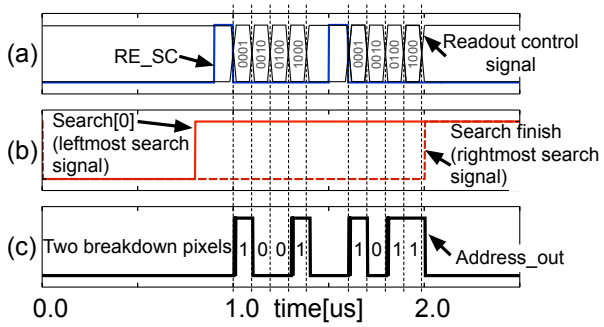


Fig. 5 Measurement results when synchronous part was operating at 10MHz.

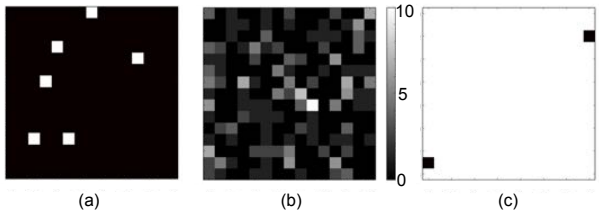


Fig. 6 Images captured when testing SPADs.