# A CMOS image sensor with lateral electric field modulation pixels for sub nano-second time response fluorescence lifetime imaging microscopy

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#### Abstract

This paper presents a time-resolved CMOS image sensor with high-speed lateral electric field modulation (LEFM) gating structure for both charge transfer and draining. A time windowed signal charge can be transferred from a pinned photo diode (PPD) to a pinned storage diode (PSD) by turning on the transfer gate pair which are situated beside the channel. This structure allows a potential barrier-less and trap-less charge transfer from PPD to PSD.

## 1. Introduction

Fluorescence lifetime imaging microscopy (FLIM) is widely used in biology. Time resolved CMOS imagers have been paid much attention to implementing a compact and low cost FLIM system, which allows to implement a next-generation endoscope. A CMOS FLIM imager using draining only modulation (DOM) pixel structure which has impulse response of 2ns has been reported [1]. To improve the impulse response, another CMOS FLIM imager using dual port LEFM gating on transfer side improves the impulse response to be 180ps [2]. However, the dual-port pixel occupies relatively large pixel area. This paper presents a CMOS imager with complete LEFM gating structure for both transfer and draining with compact pixel size and faster response. In this pixel, the storage diode is implemented for true-CDS to cancel reset noise, compared with a CMOS TOF imager without storage diode [3].

## 2. General Instructions

## Pixel structure

The LEFM pixel can implement windowed detection of fluorescence photo-electrons. Conceptual illustrations of its 3 dimensional structure and 2 dimensional potential profile are shown in Fig. 1. Buried photo diode P+/n/p-sub is formed on top of p-substrate. Like the static-induction transistor (SIT) [4], which is used in high speed applications above 2GHz, transfer gate (TG) and draining gate (TD) are situated beside the current path in LEFM structure. The potential of the channel can be influenced by the gate voltage as well as the drain voltage. During windowing the signal charge, negative gate voltage on TD lowers the channel potential and positive gate voltage on TG raises the potential, and signal charges in PPD are drifted to PSD. During draining the unwanted charges, positive gate voltage on TD raises the channel potential and negative gate voltage on TG lowers the potential, and unwanted charges in PPD are drifted to the drain. The advantage of gates situating beside the channel is no barrier and no trap exists along the transfer path, therefore, sub nano-second time response can be prospected. Because the measured fluorescent decaying is a convolution of real fluorescent decay with sensor impulse response, shortening sensor impulse response can improve measurement accuracy.



Fig. 1 3-D Structure and 2-D potential profiles along current path

Sensor Architecture



The block diagram of the FLIM sensor chip  $(512(V) \times 310(H) \text{ pixels}, 5.6 \times 5.6 \text{ um}^2)$  is shown in Fig. 2. Gating signal for controlling TD and TG are provided from top of

pixel array, feeding to all pixels through a clock tree. Each branch of the clock tree can drive one column of pixels' gating signal. Very weak photo signal from pixel are read out by analog CDS firstly. The folding integration / cyclic ADC can do multi-sampling for the amplification of the weak photo signal, and noise of pixel source follower and readout circuits are much reduced by the sampling number of 32 times [5]. The output of ADC has 18-bit codes, which then are transmitted through LVDS (Low Voltage Differential Signaling) to the output pin of chip.

Measurement method of fluorescence lifetime is the same as that discussed in [1], which is called integration measurement method. Another method is the differentiation method, which plots difference of two neighboring signal taken by integration method.

In the simulation of the impulse response, a light of short pulse width of 1ps is used instead of an impulse light. Fig. 3 shows the simulation result of time response of 374nm light pulse. The light illuminates on aperture area of PPD and the signal is obtained in PSD. The simulated impulse response using the differential method is 21ps.



Fig. 3 Simulated impulse response of 374nm light

Fig. 4 shows the measured photo charge intensity decay for 374nm laser and four kinds of fluorescent acrylic screen, using integration method in Fig. 3. An ultraviolet laser diode with a wavelength of 374nm and a pulse width of 80ps is used for both intrinsic response measurement and excitation. When measuring fluorescent screen, a laser light is illuminated on sample, the sample absorbs the laser light and emits fluorescence light, which is reflected toward the sensor by a mirror. Unabsorbed laser light is filtered out using optical band pass filter, only the fluorescence light can pass the optical band pass filter and incident into sensor chip.

Fig. 5 shows the comparison of the target lifetime and measured lifetime of Fig. 4, using LEFM pixel and DOM pixel. The device impulse response of LEFM pixel is measured to be 150ps, which is 6 times larger than the simulation result because of the influence of slow response of gating signal, but much smaller than 2ns using DOM pixel. The impulse response causes an offset for the lifetime measurement.



Fig. 4 Measured intensity decay of laser and acrylic screen



Fig. 5 Linearity of measured lifetimes

# 3. Conclusions

A time-resolved CMOS image sensor using LEFM pixels for fluorescence lifetime imaging has been implemented and evaluated. The fluorescence decaying has been successfully measured. The prototype sensor is useful for a compact and low-cost FLIM camera in biological measurements. The measured impulse response is much larger than the simulation results, this problem should be solved in future study.

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#### References

- [1] Z. Li et al, IEEE Trans. Electron Devices. 59 (2012) 2715.
- [2] M. W. Seo, Proc. Int. Symp. Solid-State Circuits Conf. (2015) 737.
- [3] S. M. Han, Proc. Int. Symp. Solid-State Circuits Conf. (2014) 130.
- [4] J. Nishizawa, IEEE Trans. Electron Devices. 22 (1975) 185.
- [5] N. Kawai, IEICE Electronics Express. 2 (2005) 379.