Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp842-843

39% tAC Improvement, 11% Energy Reduction, 32Kbit 1R/1W 2port SRAM using Two-stage Read Boost and Write-Boost after Read Sensing Scheme

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Abstract

We propose novel circuit techniques for 1R/1W 2port-SRAM to improve read access time (tAC) and write-margins at low-voltages. Two-stage read boost (TSR-BST) scheme and Write-WL boost (WWL-BST) after read sensing scheme have been proposed. TSR-BST reduces the worst read-BL delay by 61% and RBL amplitude by 10% at 0.5V, which improves tAC by 39% and reduces energy dissipation by 11% at 0.55V. WWL-BST after read sensing improves minimum operating voltage (Vmin) by 140mV. A 32kb 1R/1W 2port-SRAM with TSR-BST and WWL-BST has been developed using 40nm CMOS.

1. Introduction

Low-power SIMD processors for image processing engines are required to extend the battery life in mobile applications. In these parallel-array processors, a faster tAC, low-power 1R/1W 2port SRAMs are required as work-memories. Low-voltage operation, small-BL swing, and fast cycle time are effective for achieving such low-power SRAMs. However, as the operating voltage is reduced to near-threshold-voltage region, local variation of threshold voltage causes increase of BL delay time (tBL) and degradation of tAC. 1port Z8T-SRAM [1] and 1port complimentary read-port (C-RP) SRAM [2], both of which use differential read sensing, have been proposed to achieve fast tAC at low-voltages. However, even if these differential sensing are utilized, broad RBL delay distribution for 100mV RBL-swing at 0.5V as shown in Fig.1 limit faster tAC. Moreover, Vmin and write-time is determined by write-margins in the conventional Z-8T and C-RP 8T. Therefore, improvement of write-margins is required for low-voltage operation.

To overcome these technical issues, we propose novel circuit techniques to improve tAC and write-margins for simultaneous R/W operations at low-voltages.

2. Two-Stage Read Boost (TSR-BST) Scheme

In order to realize faster tAC, reduction of the slowest BL delay is required. Fig.2(a) and (b) show schematic and timing diagram of the TSR-BST scheme. The concept of this scheme is to reduce tBL for the slow bitcells by two-stage boosting 1) the memory cell VDD (VDDM) in the 1st-stage and 2) the selected Read-WL (RWL) driver in the 2nd-stage, dynamically. VDDM boost control is placed in every column. RWL boost control is common in each 8Rows for area-saving. In TSR-BST scheme, BSTCOL generated from internal read-clock (ICLKR) for VDDM boosting and BSTRWD generated from delayed ICLKR for RWL boosting are introduced. After SA-enable (SAE) is activated, VDDM goes down to VDD. Fig.3 shows simulated RBL delay distribution of the TSR-BST at 0.5V. The Worst tBL at -4σ is reduced by 61%. Fig.4 shows simulated RBL amplitude distribution. 10% reduction of median of RBL amplitude is confirmed by shortening SAE timing with TSR-BST. Fig.5 shows simulated waveform of the TSR-BST at 0.5V. Simulated tAC is reduced by 36%.

3. Write-WL Boost (WWL-BST) after Read Sensing for Simultaneous R/W Scheme

To improve write-margins, Write-WL boost after read sensing for simultaneous R/W scheme is developed. Fig.6 show schematic and timing diagram of WWL boost after read scheme for simultaneous R/W. WWL boost control is also common in each 8Rows. BSTWWD generated from delayed internal write-clock (ICLKW) is introduced. To realize simultaneous R/W with WWL-BST, selected WWL boost is carried out after read sensing when VDDM falls down to VDD. Simulated write time is reduced by 33% at 0.5V, -4σ as shown in Fig.7. Improvement effect of this work by simulation is summarized in Fig.8.

4. Experimental Results

A 32Kb 1R/1W 2port 8T-SRAM with TSR-BST and WWL-BST schemes has been fabricated by 40nm CMOS. Fig.9 shows a measured shmoo. Fig.10 shows a measured tAC. Fig.11 shows a write bit-error-rate (BER). Fig.12 shows energy consumption. Vmin is improved from 0.62V to 0.55V at 50ns with TSR-BST and WWL-BST. tAC is improved by 39% at 0.55V using TSR-BST. Read energy consumption with TSR-BST at 0.55V is 11.2% lower than that without TSR-BST at 0.62V. Write energy consumption with WWL-BST at 0.55V is 16.4% lower than that without WWL-BST at 0.62V. The proposed SRAM has achieved 8.3% energy reduction compared to the lowest energy consumption SRAM in the previous works as shown in Fig.13 [3-7]. 0.55V, 99fJ/access/IO-bit, 39% tAC improvement has been achieved. Fig.14 shows a die photo. Characteristics of a chip are summarized in Table 1.

5. Conclusions

TSR-BST scheme and WWL-BST after read sensing scheme have been proposed to improve access time (tAC) and write-margins at low-voltages. tAC is improved by 39% at 0.55V using TSR-BST. Read and write energy dissipations are reduced by 11.2% and 16.4%, respectively, using TSR-BST and WWL-BST. Low energy dissipation of 99fJ/access/IO-bit at 0.55V is confirmed from the measured results of SRAM with TSR-BST and WWL-BST schemes.

Acknowledgements

This work was carried out as a part of the Extremely Low Power (ELP) project supported by METI and NEDO. The authors would like to thank Prof. T. Sakurai of the University of Tokyo.

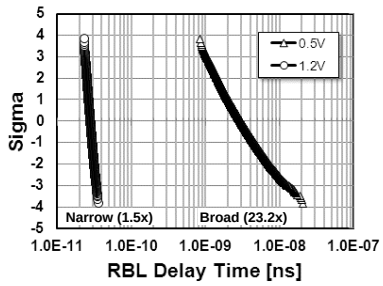

Fig.1. Conventional C-RP 8T RBL delay time distribution at V_{DD}=0.5V and 1.2V.

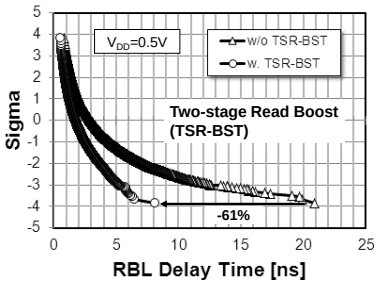

Fig.3. Simulated RBL delay time distribution of C-RP 8T at V_{DD}=0.5V.

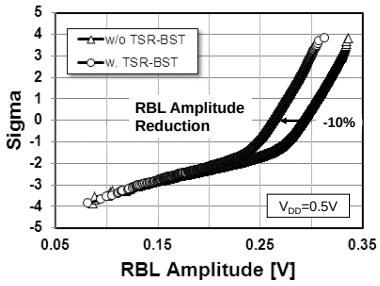

Fig.4. Simulated RBL Amplitude distribution at V_{DD}=0.5V with TSR-BST and without TSR-BST.

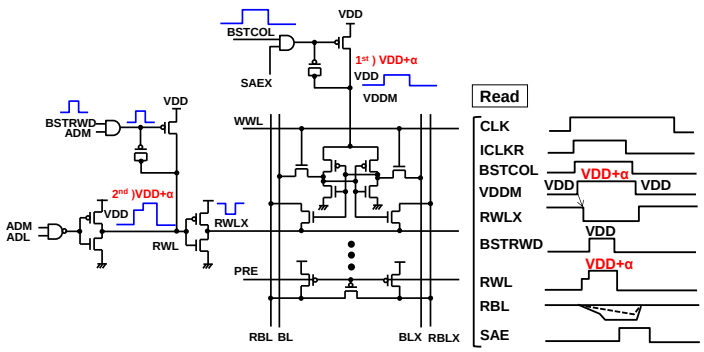

Fig.2. Two-stage Read Boost (TSR-BST) scheme (a) schematic, (b) timing diagram.

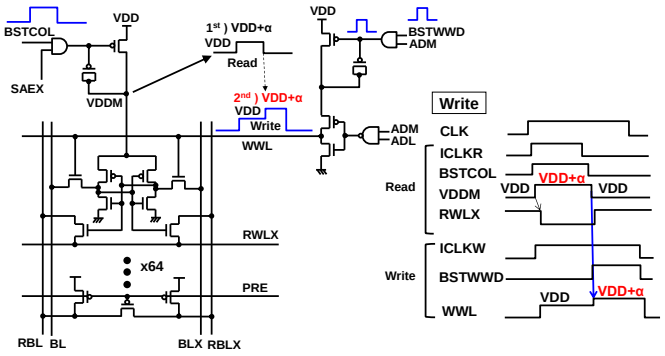

Fig.6. Write-WL Boost (WWL-BST) after read sensing for simultaneous R/W scheme (a) schematic, (b) timing diagram.

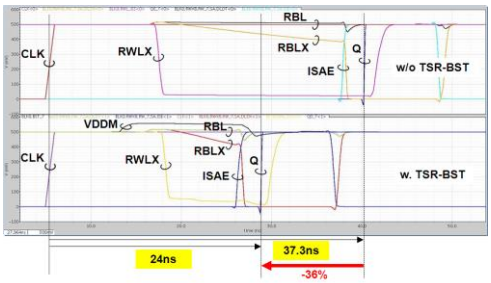

Fig.5. Simulated waveform of TSR-BST at V_{DD}=0.5V.

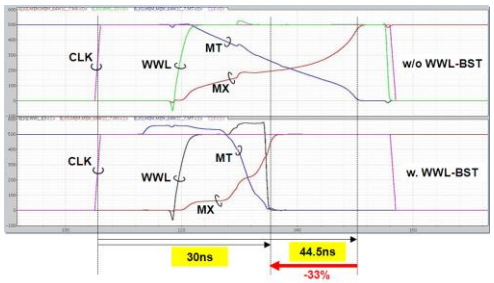

Fig.7. Simulated waveform of WWL-BST at VDD=0.5V. MT and MX are storage nodes of bitcell.

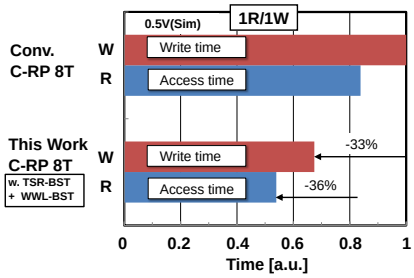

Fig.8 Improvement summary of this work. Write time is defined as CLK to SN 90% time.

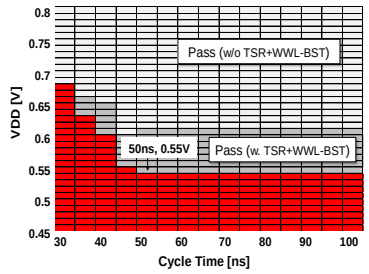

Fig.9. Measured R/W shmoo.

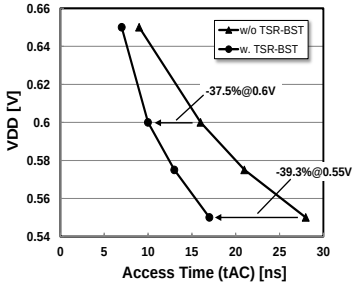

Fig.10. Measured access time.

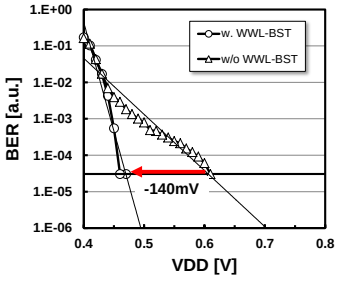

Fig.11. Measured Write-BER.

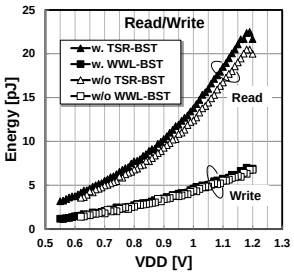

Fig.12 Measured energy consumption (2Kbit).

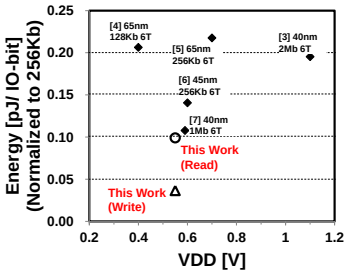

Fig.13 Comparison with previous SRAMs of energy dissipation.

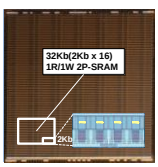

Fig.14 Die photo.

Table.1 Characteristics of test chip

Technology	**40nm LP-CMOS Process**
Cell Type	**C-RP 8T (1R/1W)**
Cell Size	**0.784μm² (Logic Rule)**
Macro Size	**162μm x 73μm (2Kb)**
Total Capacity	**32Kb**
Organization	**(64Row x 1Col) x 32bit x 16, 512I/O**
Access Time	**17ns @0.55V**
Power Consumption	**3.17pJ(R) /1.17pJ(W) (2Kb) @0.55V**

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