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Digitally Calibrated Dynamic Latched Comparator with Stochastic Offset Voltage Detection Technique for Low-Power ADCs

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Abstract

This paper presents a low offset voltage dynamic latched comparator using a full-digital calibration for low-power ADCs. The designed comparator uses a reconfigurable differential pair and the configuration is determined by digital calibration scheme to minimize its offset voltage. A detection of the offset voltage in the calibration scheme is realized by a stochastic offset detection technique. The designed comparator fabricated in a standard 0.18-μm CMOS process achieves a standard deviation of the offset voltage of 600 μV and the measured power consumption is 4.44 μW at a power supply of 1.5 V.

1. Introduction

A low-power precise dynamic latched comparator for ADCs is needed for many sensor systems, including analog frontend circuits for multi-channel arrayed sensor systems. Although a scaling of CMOS technology enables low-power operation in digital systems, an offset voltage of a comparator increases because of the MOSFET mismatch [1]. When designing an ADC, a comparator's unacceptable offset voltage degrades an ADC's effective number of bit (ENOB) [2]. Therefore, an offset reduction technique for comparators is necessary.

In conventional ways, a preamplifier is often used in front of the dynamic stage to reduce the offset voltage [3]. However, such a preamplifier consumes chip area and static power. On the other hand, a digitally self-calibrating technique named as automatic differential-pair matching (ADPM), has been reported in [4]. Fig. 1 shows a block diagram of a designed comparator with the digital calibration loop for ADPM. The offset voltage of the comparator follows the Gaussian probability distribution. In this method, a reconfigurable differential pair (RDP) that composed of some separated MOSFETs and some switches to change connectivity is introduced in the comparator's input stage. The RDP is configured to minimize the offset voltage of the comparator by calibration logic. The technique does not use any capacitors as an analog memory to hold a calibration result. Therefore, the ADPM is suitable for low-power applications. In this case, since this digitally-assisted technique has only been applied to a linear circuit like an amplifier because its ease of detection of the offset voltage during calibration, other solution is needed if a non-linear circuit like a comparator uses the ADPM for low-power realization. An offset detection technique for the dynamic latched comparator has been proposed in [5]. This technique is based on a time-domain offset detection and can be realized by full-digital circuits. However, in this technique, a time-to-digital converter (TDC) that consumes large chip area and power is required to measure a comparator's metastable time. Another offset detection technique also has been proposed in [6]. This technique is based on a stochastic method and performed in digital domain. However, this technique requires a high resolution DAC to compensate the offset voltage and a calibration processor must operate constantly in the background of using the comparator. This paper proposes full-digital offset detection technique based on a stochastic method that provides a simple digital part, resulting in small area and low-power operation.

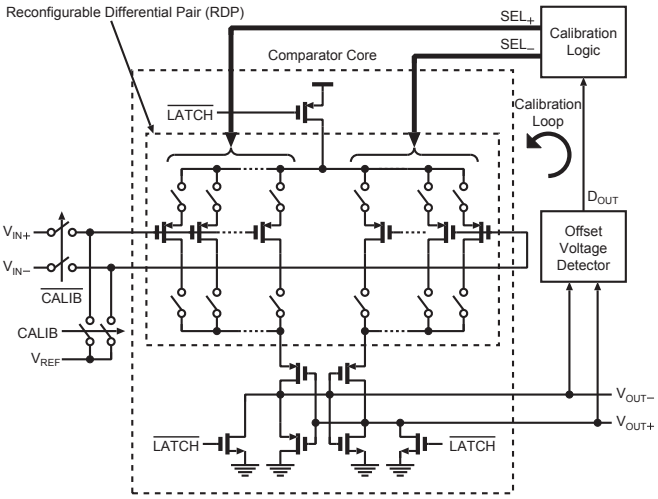

Fig. 1 Block diagram of the comparator with digital calibration loop for automatic differential-pair matching (ADPM).

2. Self-Calibrating Comparator Using A Stochastic Offset Detection

In general, result of the comparator has some uncertainly due to an input-referred noise when an input voltage of the comparator $V_{IN} = V_{IN+} - V_{IN-}$ is small. Fig. 2 shows a cumulative distribution function (CDF) of V_{IN}. If $V_{OS} = 0$, probability for $V_{OUT} = V_{OUT+} - V_{OUT-} = +1$ is 50 per-

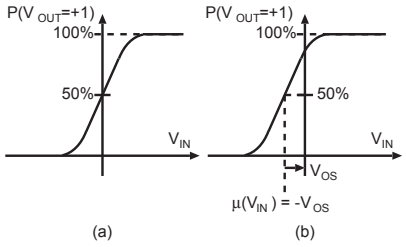

Fig. 2 Uncertainness of the comparison result by the comparator noise; (a) cumulate distribution function (CDF) of V_{IN} when $V_{OS} = 0V$; (b) CDF of V_{IN} when $V_{OS} \neq 0V$.

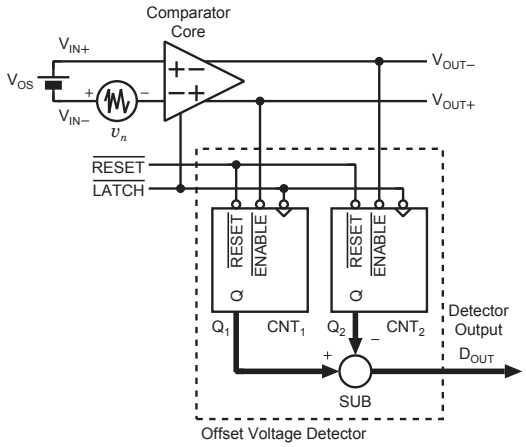

Fig. 3 Block diagram of the proposed stochastic offset voltage detector.

cent at $V_{IN} = 0V$ [Fig. 2(a)]. When $V_{OS} \neq 0$, an mean of the CDF $\mu(V_{IN})$ shifts from 0V to $-V_{OS}$ [Fig. 2(b)]. Therefore, V_{OS} can be detected by measuring a probability for $V_{OUT} = +1$ at $V_{IN} = 0V$. The proposed technique can be easily realized by some basic digital components.

Fig. 3 shows block diagram of the proposed stochastic offset detector. The detector consists of two binary counters (CNT_1, CNT_2) and a subtractor (SUB). Two inputs of the detector are connected to output terminals of the comparator V_{OUT+}, V_{OUT-}. CNT_1 counts up when $V_{OUT+} = +1$. CNT_2 also counts up when $V_{OUT-} = +1$. In the calibration mode, two input terminals of the comparator V_{IN+},V_{IN-} are shorted and the resulting input voltage of the comparator is $V_{IN} = V_{OS} + v_n$. The comparator outputs a random bit stream that follows the Gaussian probability distribution. When measurement starts, CNT_1 and CNT_2 are reset to zero. These counters operate in synchronization with comparator latch signal $\overline{LATCH}$ and count an each bit stream of V_{OUT+}, V_{OUT-}. Finally, resulting probability corresponding V_{OS} (D_{OUT}) can be obtained by SUB that outputs a difference between Q_1 and Q_2. If $V_{OS} > 0$, then $D_{OUT} > 0$. In contrast, $D_{OUT} < 0$ if $V_{OS} < 0$. If the absolute value of V_{OS} is small, D_{OUT} approaches zero. The calibration logic shown in Fig. 1 configures the RDP to minimize the absolute value of D_{OUT}.

3. Measurement Results

18 prototypes of the proposed comparator have been fabricated in 0.18-μm CMOS process. The chip microphotograph

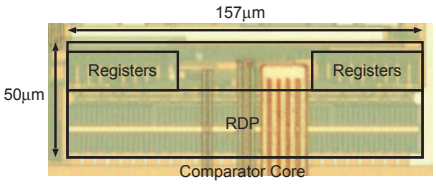

Fig. 4 Chip microphotograph.

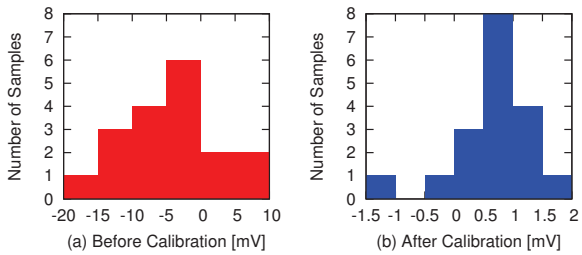

Fig. 5 Measured input-referred offset voltage; (a) before and (b) after calibration.

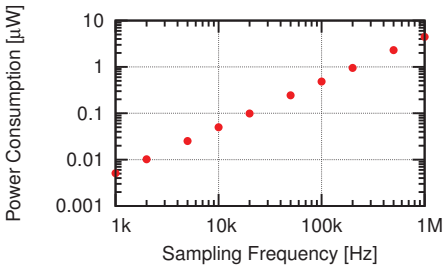

Fig. 6 Measured power consumption as a function of sampling frequency after calibration.

of this prototype is shown in Fig. 4, the die area of which is 157 μm $\times$ 50 μm. The prototype chip architecture is based on Ref. [5] that is composed of the comparator core with the RDP and registers for interface to an external MCU. In this design, the proposed offset detector and the calibration logic are implemented by the external MCU. The histogram of the input-referred offset voltage is shown in Fig. 5. It is confirmed that the standard deviation of offset voltage $\sigma(V_{OS})$, is improved from 7.05 mV to 600 μV, which can be achieved by using the proposed detector and calibration scheme based on the ADPM. Measured power consumption of the comparator is 4.44 μW at 1 MHz sampling frequency is shown in Fig. 6. Therefore, the proposed stochastic offset detection technique is suitable for low power ADCs.

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