Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp880-881

Selective epitaxy of Ge on nano-tip patterned Si (001): towards defect-free Ge islands

Gang Niu[1*], Giovanni Capellini[1,2], Tore Niermann[3], Marco Salvalaglio[4], Anna Marzegalli[4], Markus Andreas Schubert[1], Peter Zaumseil[1], Hans-Michael Krause[1], Oliver Skibitzki[1], Michael Lehmann[3], Francesco Montalenti[4], Ya-Hong Xie[5], Thomas Schroeder[1,6]

1 IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany
Phone: +49-335-5625-378 E-Mail: gang@ihp-microelectronics.com
2 Dipartimento di Scienze, Università Roma Tre, Viale Marconi 446, 00146 Rome, Italy
3 Technische Universität Berlin, Institut für Optik und Atomare Physik, Straße des 17. Juni 135, 10623 Berlin, Germany
4 L-NESS and Dept. of Materials Science, Università degli Studi di Milano-Bicocca, via Cozzi 55, Milan, Italy
5 University of California at Los Angeles, Dep. of Materials Science and Engineering, Los Angeles, CA 90095-1595, USA
6 BTU Cottbus-Senftenberg, Konrad-Zuse-Str.1, 03046 Cottbus, Germany

Abstract

Defect-free Ge islands are very attractive for various electronic and optoelectronic devices. In this report, we demonstrate wafer-scale integration of relaxed Ge islands on up to 4 inch size Si (001) substrate via Si nano-tips. The Si-tips patterned substrate is fabricated by CMOS compatible nanotechnology and features nanometer size Si seeds regularly emerged in a SiO_2 matrix. The mechanism of pattern-independent selectivity is discussed in detail. Elevated temperatures (>750°C), required to realize selective growth, assure high crystallinity quality of the Ge islands while it does not induce strong Si intermixing in Ge islands due to the specific geometry of our nano-tip patterned wafers. Both experimental and theoretical results suggest that such Ge nano-islands can be entirely elastically relaxed and it is thanks to local intermixing acting around the Si tip that allows a delay in plastic relaxation. Such well-ordered Ge-rich islands with low defect density could certainly help to improve the performance of Ge based nano-devices.

1. Introduction

High quality Ge selectively grown on Si is becoming more and more interesting for a wide spectrum of electronic and optoelectronic applications such as high-mobility complementary metal-oxide-semiconductor (CMOS) transistors[1]; tunnel field-effect transistor (TFET) where low defective interfaces between lattice mismatched materials are keys for steep slope operation[2]; Si-based III-V multi-junctional solar cells[3]; and monolithic integration of photonics with CMOS technology[4]. However, the relatively large lattice mismatch and thermal expansion coefficient (TEC) mismatch make it a quite challenging to realize defect-free Ge materials on Si. Furthermore, the Ge-Si interdiffusion causes difficulty in the control of the resulting heterostructure. Selective nanoheteroepitaxy (NHE) has been demonstrated to be able to prevent plastic relaxation in Ge nano-islands. NHE, which was initially developed by Luryi et al.[5] and Zubia et al.[6, 7] is based on selective growth and attracts intense research interests. According to NHE theory, the critical thickness of growing films in lattice-mismatched hetero-epitaxial systems can be increased by reducing the lateral dimension of the Si seed pads, eventually leading to dislocation-free epitaxial materials given the seed pads size is sufficiently small. NHE offers advantages including i) pure elastic relaxation of mismatch strain in three dimensions; ii) isolated seeds avoid cracking or wafer bowing due to thermal mismatch and iii) compliance effects permitting strain partitioning. Our group has demonstrated the successful NHE of high quality Ge on different types of patterned Si wafers including Si nanopillars[8-11] or Si compliant nanomesas[12, 13] etc. Defect-free Ge nano-islands have been recently achieved on free-standing Si nanomesas and the compliance of the growth approach was proved by the strain partitioning between the epitaxial Ge and the Si substrate nanostructure[14]. Nevertheless, a SiGe intermediate layer is indispensable to be interposed between Ge and Si to eliminate the misfit segments thus realizing coherent Ge.

In this report, we demonstrate a new technique, namely, selective growth of Ge on nano-tip patterned Si (001) substrates by molecular beam epitaxy (MBE), which enables fully coherent Ge islands. We will discuss in detail the selectivity mechanism of Ge and key impacts of growth temperature and growth rate. We will show that the high temperature required to achieve perfect selectivity and good crystalline quality, does not lead to extensive Ge-Si intermixing. Only limited intermixing is observed, which is confined to the island pedestal region resulting in all Ge islands having composition of ~95% Ge when averaged over the entire Ge volume. Moreover, thanks to the strain partitioning between Ge and Si tips, the thin intermixing layer has a beneficial role to prevent the formation of misfit dislocations (MDs) at the advantage of a fully elastic relaxation. We shall see the key enabler of this peculiar growth mode is the shape and size of the patterned Si substrate used as “seed” for the selective epitaxy.

2. Experiments

The nano-tip patterned Si (001) wafers were fabricated using standard 130 nm CMOS lithography technology[15]. Fig. 1 shows the wafer structure with schematic and scanning electron microscopy (SEM) images. The Si tips are arranged in a two-dimensional square array with tip-tip spacing (d) being 0.5μm to 2 μm and tips are surrounded by SiO_2. Chemical-mechanical polishing (CMP) was carried out to expose the crystalline Si seeds of ~50 nm diameter. It is noted that the duration of the CMP step can be used to control the surface area of the crystalline Si seed openings (with a minimum of ~5 nm in diameter) and thus the nucleation size for subsequent Ge heteroepitaxy. After chemical cleaning by HF and a pre-baking at a substrate temperature of 850°C for 5 min, the Ge growth was performed in a DCA MBE chamber. A comprehensive study on the morphology, crystallinity, strain and the interface of Ge nano-islands was performed by using techniques including atomic force microscopy (AFM), lab- and synchrotron radiation- based X-ray diffraction (XRD), micro-Raman (μ-Raman) and transmission electron microscopy (TEM). Linear elasticity calculations by Finite-element method (FEM) was employed to calculate the strain status in a Ge/Si-tip structure to demonstrate its coherency and study the elastic relaxation details.

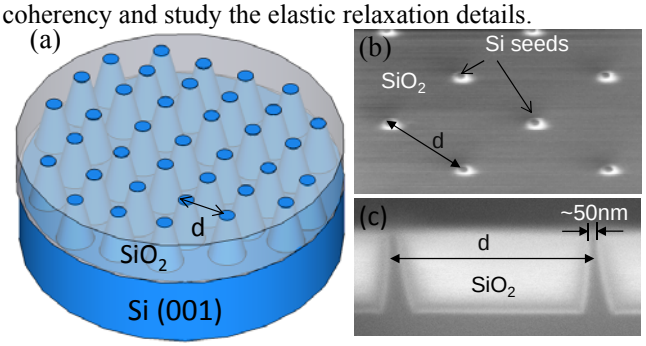

Fig. 1 Nano-tip patterned Si wafers: (a) schematic image; (b) plane view and (c) cross-sectional view SEM images. The tip-tip distance d ranges from 0.5μm to 2μm.

3. Results

The MBE growth of Ge on tip-patterned wafers was carried out at different temperatures (500°C-850°C) and Ge growth rate (8-22ML/min) and it is found that higher temperature and low growth rate lead to better selectivity. Particularly, under optimized growth conditions, perfect selectivity was obtained, as shown in the SEM image in Fig. 2 (a). According to the out-of-plane and in-plane XRD measurements shown in Fig. 2 (b), Ge islands are almost fully relaxed with slightly smaller lattices (-0.01%), which is probably due to Si interdiffusion. Fig. 2 (c) reveals a high resolution TEM (HRTEM) cross-sectional image of a Ge island grown on a Si tip at 850°C. One observes neither dislocation networks nor other defects, thanks to the nm-size Si seeds and fully elastically relaxation of Ge. The top of the Si tip deforms with a "hole" region filled by Ge, which is due to the high pre-baking and growth temperature. EDX image shown in Fig. 2 (d) demonstrates more clearly this deformation. It also reveals a slight Si interdiffusion into the Ge island (95% Ge) and the intermixing is confined at the pedestal part of the Ge island. FEM simulation (not shown) suggests that the thin SiGe layer at the interface plays a significant role in realizing fully coherent Ge islands on Si nano-tips.

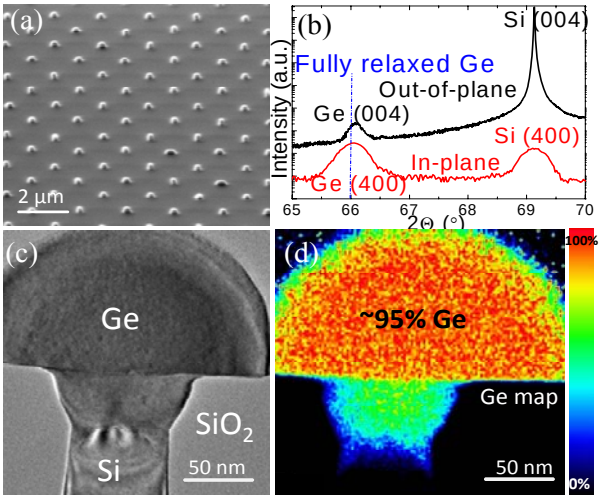

Fig. 2 (a) A SEM plane view image showing the highly selective growth of Ge on Si-tip substrate with a tip-tip distance of ~1.4μm; (b) Out-of-plane (black) and in-plane (red) lab-based XRD results; (c) HRTEM cross-sectional image of a Ge island on a Si tip and (d) TEM-EDX image on the same heterostructure in (c).

4. Conclusions

Fully coherent, well-ordered Ge islands were selectively grown on nano-tip patterned Si (001) by MBE. The particular selectivity mechanism leads to pattern-independent selectivity. The shape and size of Si patterned substrate and the local SiGe intermixed layer, occurring at the pedestal region of the Ge island, lead to completely elastic relaxation of Ge. High growth temperatures (>750°C) are required for growth selectivity but a "geometric intermixing hindrance" effect of the Si-tip wafer confines intermixing to the pedestal region. One observes neither dislocation networks at the Ge/Si interface nor other defects like twins or stacking faults in the volume of the Ge nano-structure. Such high quality Ge nano-islands will facilitate the improvement of the performances of both electronic and optoelectronic Ge related devices.

References

[1] M. L. Lee, *et al. J. Appl. Phys.* **97** (2005) 011101.
[2] A. M. Ionescu and H. Riel. *Nature* **479** (2011) 329-337.
[3] J. M. Olson, *et al.*, High-Efficiency III-V Multijunction Solar Cells. In *Handbook of Photovoltaic Science and Engineering.*, 2nd ed.; Luque, A.; Hegedus, S., Eds. John Wiley & Sons: 2010; pp 360-408.
[4] J. Wang and S. Lee. *Sensors* **11** (2011) 696-718.
[5] S. Luryi and E. Suhir. *Appl. Phys. Lett.* **49** (1986) 140-142.
[6] D. Zubia and S. D. Hersee. *J. Appl. Phys.* **85** (1999) 6492-6496.
[7] D. Zubia, *et al. J. Vac. Sci. Tech. B* **18** (2000) 3514-3520.
[8] G. Kozlowski, *et al. Appl. Phys. Lett.* **99** (2011) 141901.
[9] P. Zaumseil, *et al. J. Appl. Phys.* **109** (2011) 023511.
[10] G. Kozlowski, *et al. Nanotechnology* **23** (2012) 115704.
[11] P. Zaumseil, *et al. Nanotechnology* **23** (2012) 355706.
[12] P. Zaumseil, *et al. J. Appl. Phys.* **112** (2012) 043506.
[13] P. Zaumseil, *et al. J. Appl. Cryst.* **46** (2013) 868-873.
[14] F. Montalenti, *et al. Phys. Rev. B* **89** (2014) 014101.
[15] W. Mehr, *et al. Microelectron. Eng.* **30** (1996) 395-398.