Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp914-915

Pseudo-CMOS Gain Enhancement by Post-Annealing Organic Circuits on Ultrathin Plastic Substrates

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Abstract

We report on the design and fabrication of circuit level integration of thermally stable short channel organic transistors on 1 μm parylene substrates. With channel lengths below 5 μm, single transistors can maintain bandwidth of 100 kHz even after annealing at 150°C. Using short channel transistors, we realized pseudo-CMOS inverters and improved their gain by at least 150% with a simple post-annealing process. Significant improvement in gain value was consistent for devices with different architectures. Short channel circuit fabrication with high thermal stability and improved gain is an important step towards practical application of imperceptible electronics.

1. Introduction

Organic thin-film transistors (OTFTs) are attractive circuit elements to realize the next generation of flexible electronics devices. Advancements in material science allowed organic semiconductors to present better and more reliable performance for circuit level integration. In addition, organic transistors can be thermally stable up to very high temperatures [1]. Recently an important progress was demonstrated by reducing substrate thickness down to only 1 μm thick plastic substrate to improve OTFTs' flexibility and weight per area [2]. Nevertheless, a demonstration of short channel transistors and circuits with good thermal stability has not been realized yet on ultrathin films.

Here we present the successful fabrication of short channel, bottom contact transistors and circuits on ultrathin plastic foils that present good frequency response and thermal stability. Out material selection and process allow the devices to maintain bandwidth of 100 kHz even after post-annealing at 150°C. Moreover we show how we can enhance inverters performance significantly by a simple thermal treatment. The utilization of short channel transistors allows circuits to improve gain and maintain their frequency response at high temperatures.

2. Experiment

Fabrication process

In Fig. 1a we present the transistors bottom contact architecture on ultrathin films. The ultrathin parylene diX-SR substrate was vapor deposited on a sacrificial Si/SiO_2 wafer. Photolithography was used for fine patterning of source and drain (Fig. 1b). Gold contacts were modified by pentafluorobenzenethiol (PFBT) to improve transistor performance and reduce contact resistance in the bottom contact structure [3]. Air stable dinaphtho[2,3-b:29,39-f] thieno[3,2-b]thiophene (DNTT) [4] was thermally evaporated as the organic semiconductor and 100 nm parylene diX-SR was vapor deposited as the gate dielectric.

3. Results

Cutoff frequency evaluation

Transistors were thermally annealed and measured up to 170°C. Their cutoff frequency was calculated by

$$f_T = \mu(V_{GS} - V_T) \Big/ 2\pi L(L + 2L_C) \quad (1)$$

where μ is the device saturation mobility and L, L_C are the channel length and gate-source overlap respectively. In Fig. 1c we show that the cutoff frequency of the short channel transistors (L=4 μm) is kept above 100 kHz after annealing at 150°C. For comparison we also plot the long channel transistor case (L=48 μm), fabricated in the same technology, that present inferior performance.

Pseudo-CMOS inverters gain enhancement

We fabricated ultrathin pseudo-CMOS organic inverters using transistors with 3.5 μm and different channel width ratios ($\alpha=W_2/W_1$). In Fig. 1d we illustrate the Pseudo-D inverter design [5], denoting the channel widths notation. W1 was 1500 μm in all cases. We annealed the inverters up to 150°C and plot a representative transfer characteristics of device with α=6 with changing post-annealing temperature in Fig 1e. A clear increase in gain was observed at 150°C. We evaluated inverters with various α values (α=3, 6 and 10) and plot their gain development as a function of temperature. We observed that inverter gain can be enhanced by at least 150% after simple post annealing procedure, regardless of the sizing ratio.

4. Conclusions

An increase of pseudo-CMOS inverter's gain by at least 150% after post annealing was achieved. The utilization of short channel transistors for this inverter allows significant gain increase with keeping circuit's bandwidth at 100 kHz.

Transistors and circuits show reliable and high performance even at elevated temperatures up to 150°C.

Acknowledgements

This work is partly supported by the Outstanding Graduate School Program "Secure-Life Electronics" sponsored by the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan. A.R thanks the support from the SEUT Program of Graduate School of Engineering, University of Tokyo and the financial contribution of ISEF foundation to this research. We appreciate the useful discussions of Dr. Hiroshi Fuketa and Mr. Naoji Matsuhisa regarding circuit and device analysis.

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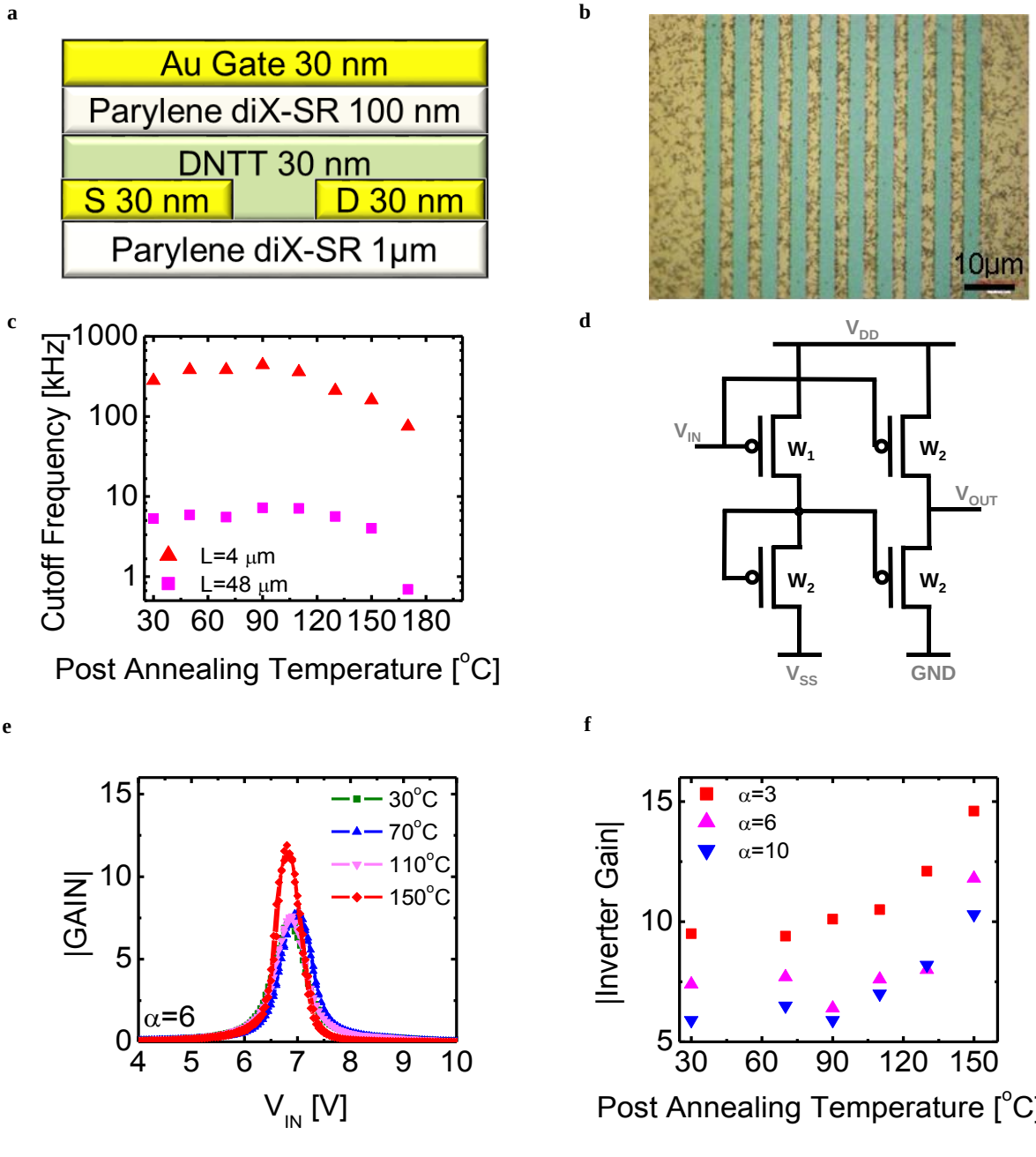

Figure 1: (a) OTFT bottom contact architecture on ultrathin films. (b) Microscopic image of short channel transistor with channel length of 3.5 µm and W/L of 1200. (c) Cutoff frequency calculation of short and long channel transistors. PFBT untreated device is also plotted for comparison. (d) Illustration of pseudo-CMOS inverter circuit on ultrathin films. (e) Transfer characteristics and inverter gain of pseudo-CMOS circuit with α=6. (f) Gain enhancement of pseudo-CMOS circuits with different sizing ratio as a function of post-annealing temperature.