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STDP behavior realization in $BiFeO_3$-based artificial synapses with short and simplified spike sequences

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Abstract

Memristive devices are popular in the past decades for their ability to emulate different forms of spike-driven synaptic plasticity by applying specific voltage waveforms at their two terminals. In this work, we investigate spike-timing dependent plasticity (STDP) with a simplified single pairing of one presynaptic voltage spike and one postsynaptic voltage spike in a $BiFeO_3$ (BFO) memristive device. We show that the analog resistive switching of the BFO-based artificial synapse allows to adjust the learning time constant of the STDP function as short as 125µs. As the power consumption is a major constraint in neuromorphic circuits, the energy-efficient setting process has also be demonstrated for BFO-based artificial synapse with short and simplified spike sequences (4.5 pJ).

1. Introduction

Spike timing dependent plastisity (STDP) opens a new avenue for understanding information coding and circuit plasticity that depends on the precise timing of neuronal spikes. Various artificial synapses have shown STDP. Numerous theoretical studies have explored the functional implications of STDP. However, the circuit- oriented approach is followed with the problems such as high circuit complexity [2, 3] and high energy consumption [4]. Therefore, nonvolatile analog resistive switches (ReRAM) responding to well-defined input signals by suitably changing their internal state ('weight') are currently developed. Polycrystalline $BiFeO_3$ (BFO) based memristors [5], as a promising ReRAM candidate, are attracting much attention due to their excellent nonvolatile bipolar, electroforming free resistive switching with long retention at higher temperature and large endurance.

On the BFO artificial synapses we have shown earlier that STDP and triplet plasticity with learning windows on the millisecond time scale can be faithfully emulated by applying 60-80 pairings of pre- and postsynaptic spikes [6, 7]. In this work instead of 60-80 pairing input signal we develop a single pairing spike order, which can significantly wider the range of timescale configurability of STDP behavior, i.e. 125µs. In order to reduce power consumption and speed up our experiments, we have increased the programming voltage slightly, enabling us to move from the usual biology-like 60-80 spike pairing STDP experiments to single pairing STDP experiments exhibiting the same kind of weight/memristance change.

2. Single pairing spike sequence and STDP diagram

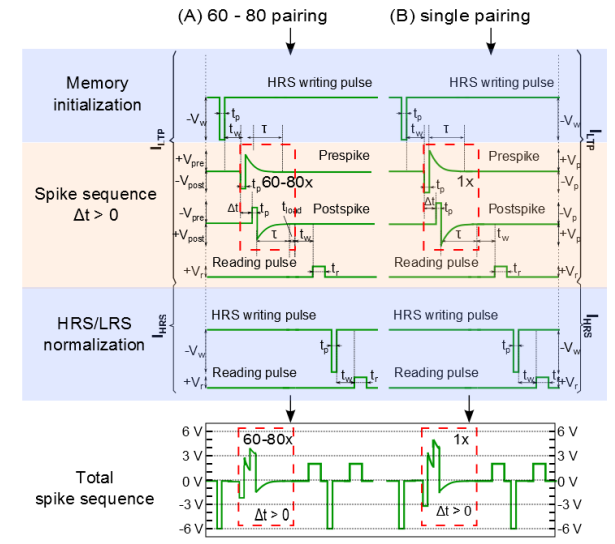

Fig. 1. Signal scheme of pre-post spike (Δt>0) for STDP emulation with (A) 60- 80 pairing spike sequence (B) a single pairing spike sequence. The potentiation current I_{LTP} and the initial HRS current I_{HRS} are used to normalize the long term potentiation current ΔI_{LTP} as defined in Eq. (1). t_p is the pulse width and t_w is the measurement waiting time before applying the reading pulse V_r.

It has been illustrated in our previous work how the 60-80 pairing pre- and postsynaptic waveforms of a specific biology-derived synaptic plasticity rule [8] can be used or adjusted to operate BFO-based memristive devices [6] (Fig. 1A). In order to shorten the total pairing spike time, we slightly increased the pre and post amplitude to $V_p = V_{pre} = V_{post} = 3.0$ V and applied a single pairing pre- and postsynaptic spike to the top and bottom electrodes of device (Fig. 1B). Both 60-80 pairing together with simplified single pairing signal scheme for potentiating

input signal ($\Delta t > 0$) are illustrated in Fig. 1. For the pulse order leading to potentiation, the step labeled Memristor initialization refers to the application of a writing pulse to set the BFO memristor into HRS, while in depressing spike sequence refers to the setting process into LRS. After the waiting time t_w, in the single pairing input signal in Fig. 1B: a single pre- and a single postspike are applied to the top electrode of device. As shown in Fig. 1 each pre- and postspike consists of one rectangular pulse with pulse amplitude V_p and one exponentially decaying pulse V_{exp}

$$V_{exp} = |V_p| \bullet exp\left(\frac{-t}{\tau}\right), \quad (1)$$

with the decay time $\tau = \tau_{pre} = \tau_{post}$, where τpre and τpost are the exponential decay times of pre- and postspikes, respectively. Here, we choose $\tau = 2.5 \cdot t_p$. The pre- and postspikes superimpose at the BFO memristor, and the spike timing difference Δt determines the waveform of the total spike. For the potentiating (depressing) spike order, the spike timing difference Δt between the pre- and postspike is positive (negative) and lies in the range: $tp \leq |\Delta t| \leq 10 \cdot t_p$.

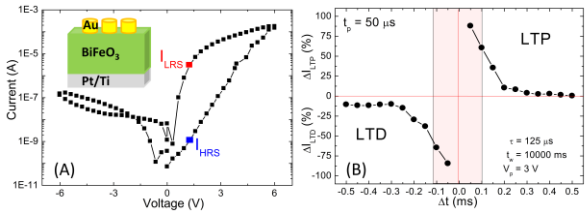

Fig. 2 (A) Hysteretic current-voltage (IV) characteristics of a Au/$BiFeO_3$/Pt memristor with a top electrode area of 4.5E4 μm^2. Inset shows the structure of a BFO memristor. (B) Long term depression current ΔI_{LTD} (negative range of y-axis) and long term potentiation current ΔI_{LTP} (positive range of y-axis) for single pairing STDP with pulse width $t_p = 50$ µs.

After the measurement waiting time t_w the synaptic weight of BFO-based artificial synapses has been checked by applying a reading bias of $V_r = +2.0$ V with a pulse width of $t_r = 100$ ms. The reading current is defined as the potentiation current I_{LTP} (depression current I_{LTD}) after sourcing potentiating spike (depressing spike).

Finally, the reading current I_{HRS} (I_{LRS}) of BFO in HRS (LRS) is recorded at a reading bias of $V_r = +2.0$ V after recording I_{LTP} (I_{LTD}). For biological reasons in order to keep STDP bounded, the LTP and LTD current values are normalized as follows:

$$\Delta I_{LTP}(\%) = \frac{I_{LTP} - I_{HRS}}{I_{LTP}} * 100\%, \quad (2)$$

$$\Delta I_{LTD}(\%) = \frac{I_{LTD} - I_{LRS}}{I_{LRS}} * 100\%. \quad (3)$$

According to the input signal scheme (Fig. 1) the BFO memristor is set in the HRS with a writing pulse amplitude of $V_w = -6.0$ V. By applying the sweeping source voltage from 0 V -> -6.0 V -> +6.0 V -> 0 V between the Au top electrode and the Pt bottom electrode, the current-voltage characteristics in BFO memristors (Fig. 2A) reveal reproducible nonvolatile hysteretic bipolar resistive switching [5]. This IV curve proves that the BFO memristor with multilevel resistive switching can be considered as an analog resistive switch and used as an artificial synapses. For the single pairing STDP measurements on a BFO-based artificial synapse the single spike pairing input signal allows us to shorten the total spike time and to adjust the learning time constant of the STDP function down to 125 µs ($t_p = 50$ µs) as shown in Fig 2B. Pulse amplitude of $|\pm V_p| = 3.0$ V and a waiting time t_w of 10 s have been chosen here. The synaptic weight of the BFO memristor scales with the normalized potentiation current ΔI_{LTP} and the normalized depression current ΔI_{LTD}. If the prespike precedes the postspike ($\Delta t>0$) biological synapses undergo long term potentiation LTP, i.e. the connection between two neurons becomes stronger. On the other hand, if the postspike precedes the prespike ($\Delta t<0$), biological synapses undergo long term depression LTD, i.e. the connection between two neurons becomes weaker. And this kind of weight changing is in a fashion similar to biology.

3. Conclusions

In this work we have developed a single pairing spike sequence for STDP measurements. Using BFO-based artificial synapses the STDP behavior with learning time constant 125µs has been investigated. During the STDP measurement the increased programming voltage helps to shorten the total pairing spike time, and enables to move from the standard biology-like 60-80 spike pairing STDP experiment to a single pairing STDP experiment with the same weight/memristance change and tremendously reduced energy consumption.

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