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Turn-on Analysis of Si-IGBTs with Emitter Trenches

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1. Introduction

A trench gate connected to the emitter electrode (emitter trench) has been widely used to suppress bus voltage oscillation under a short circuit condition [1]. Recently, optimization of carrier distribution with an emitter trench for high speed switching has been proposed [2-3]. Hence, the emitter trench plays a crucial role in improvement of the short circuit capability and turn-off characteristics. However, the effects of the emitter trench on the turn-on characteristics have not yet been made clear.

This study reports on the turn-on analysis of Si-IGBTs with emitter trenches. The tail of the collector-to-emitter voltage (V_{CE} tail) during turn-on fluctuated when an emitter trench was inserted. Interestingly, the gate-to-collector capacitance of IGBTs with an emitter trench was less than that without an emitter trench. From this device simulation, it became clear that this V_{CE} tail variation derives from decrease in the PNP gain associated with the change in the hole current path.

2. Experiments

The inset of Figure 1 shows the simulated IGBT with an emitter trench. Main and emitter trenches had the same geometry except for the connection terminal. Turn-on waveforms with an inductive load were calculated. All simulations were carried out using the Sentaurus Device.

3. Results and Discussion

Figure 1 shows the turn-on waveforms of IGBTs with and without an emitter trench. The gate resistance (R_G) in each IGBT was adjusted to coincide with turn-on di/dt. The insertion of an emitter trench made a difference in the V_{CE} tail. Figure 2 shows the mesa width (between main and emitter trench, "W_{mesa}") dependence of the time to reach to the 10% V_{CE} (T_{CE}). The V_{CE} tail lengthened as the emitter trench got closer to the main trench. In contrast, the V_{CE} tail was almost independent of W_{mesa} in the case where an emitter trench was connected to a gate. In general, the time variation of V_{CE} (dV_{CE}/dt) strongly depends on the gate-to-collector capacitance (C_{GC}) [4]. Figure 3 shows a comparison of the voltage-capacitance curves of IGBTs with and without an emitter trench. C_{GC} of IGBTs is lower with an emitter trench than that without an emitter trench.

These simulated results mean that the device capacitance does not account for V_{CE} tail variation. In order to clarify the origin of V_{CE} tail variation, the internal dynamics of IGBTs with emitter trenches during turn-on was investigated. Figure 4 shows the hole current distribution of IGBTs (a) without an emitter trench, (b) with an emitter trench (with wide W_{mesa}) and (c) with an emitter trench (with narrow W_{mesa}) at the time of V_{CE} tail. The hole current path to the emitter veers close to the emitter trench as W_{mesa} narrows. This is due to lowering in the electrostatic potential around the emitter trench. Figure 4 (d) clearly shows that the hole current path becomes straight when an emitter trench was connected to a gate. We assumed that the above V_{CE} tail variation is attributed to these differences in the hole current path.

Turn-on dV_{CE}/dt can be expressed as follows:

$$\frac{dV_{CE}}{dt} = -\frac{V_{GE} - \left[V_{TH} + \left(1-\alpha_{PNP}\right) I_L / g_{MOS}\right]}{R_G C_{GC}} \qquad (1)$$

Note that dV_{CE}/dt depends not only on a time constant ($R_G C_{GC}$) but also on a parasitic PNP transistor gain (α_{PNP}). α_{PNP} can be given by:

$$\alpha_{PNP} = \gamma_e \alpha_T = \left(1 + \frac{\sigma_B}{\sigma_E}\frac{W_B}{L_h}\right)^{-1} \alpha_T \qquad (2)$$

where σ_E corresponds to the conductivity of the p-body region. According to equations (1) and (2), decrease in σ_E leads to decrease in α_{PNP}, which in turn results in smaller dV_{CE}/dt. Since σ_E is inversely proportional to the length of hole current path in the p-body region, the above detour may cause the decrease in α_{PNP}. To verify this hypothesis, we estimated the emitter injection efficiency γ_e near the bottom of the main trench as shown in Figure 5. γ_e is defined as the ratio of electron current to total current as also depicted in Figure 5. As expected, γ_e decreases drastically as W_{mesa} narrows. Therefore, we conclude that V_{CE} tail variation by the insertion of an emitter trench causes a detour in the hole current path.

Multiple emitter trenches need to be inserted to improve short circuit capability. In this case, however, a significant V_{CE} tail variation occurs as seen in Figure 6 (a). We propose that the emitter trench placed nearest to the main trench should be connected to a gate instead of an emitter as shown in Figure 6 (b). Owing to straight hole current flow, high speed dV_{CE}/dt comparable to that without an emitter trench can be realized.

4. Conclusions

The origin of V_{CE} tail variation during turn-on in Si-IGBTs with an emitter trench was investigated. It was found that hole current to the emitter deviates from the straight path with an emitter trench. This leads to decrease in PNP current gain, which in turn results in smaller dV_{CE}/dt. We demonstrated that this V_{CE} tail variation can be suppressed by connecting the emitter trench to a gate.

References

[1] Y. Tomomatsu *et. al.*, Proc. IAS'01, pp. 1060, 2001.

[2] R. Gejo *et. al.*, Proc. ISPSD'14, pp. 99, 2014.

[3] S. Machida *et. al.*, Proc. ISPSD'14, pp. 107, 2014.

[4] Y. Onozawa *et. al.*, Proc. ISPSD'05, pp. 207, 2005.

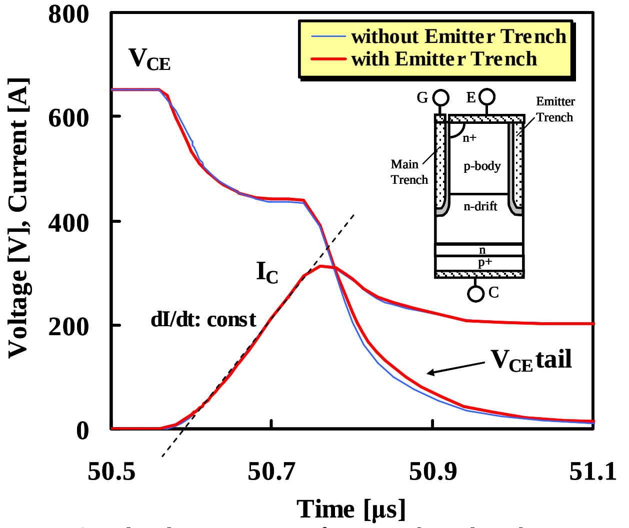

Fig. 1 Simulated turn-on waveforms with and without emitter trench.

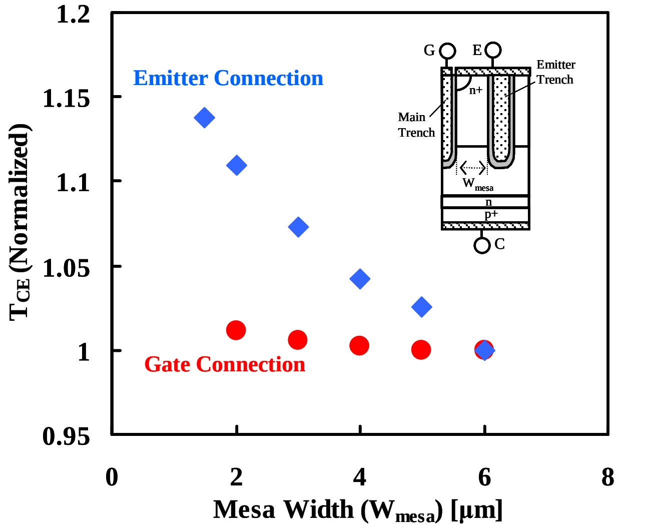

Fig. 2 Mesa width dependence of time to reach to 10 % voltage with different connection.

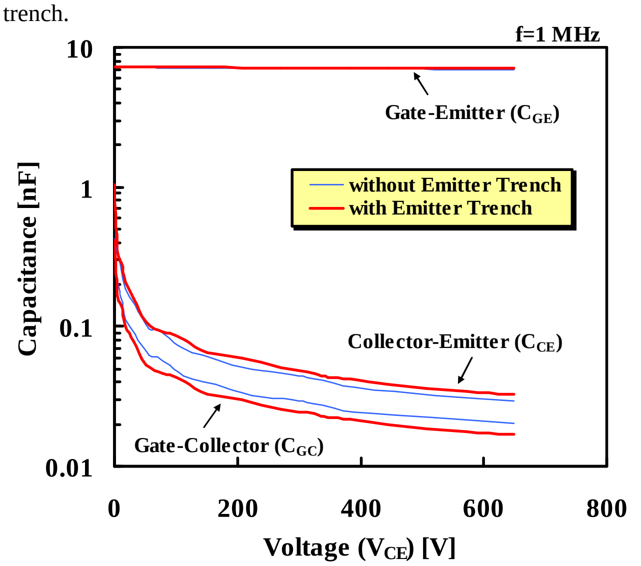

Fig. 3 Capacitance-Voltage curves with and without emitter trench.

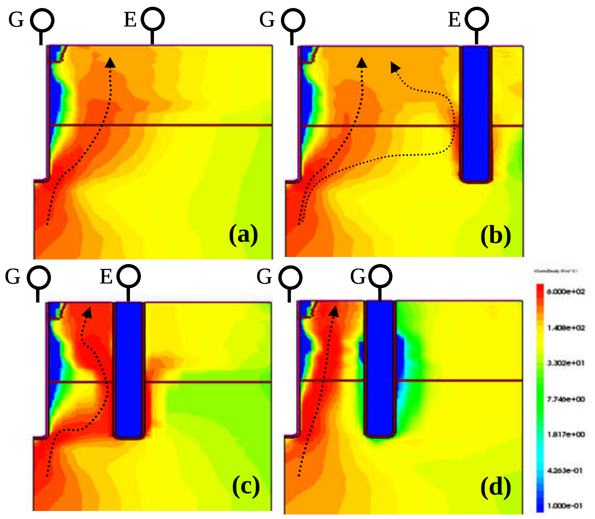

Fig. 4 Hole current distribution during turn-on (a) without emitter trench (b) wide mesa (c) narrow mesa (d) gate connection.

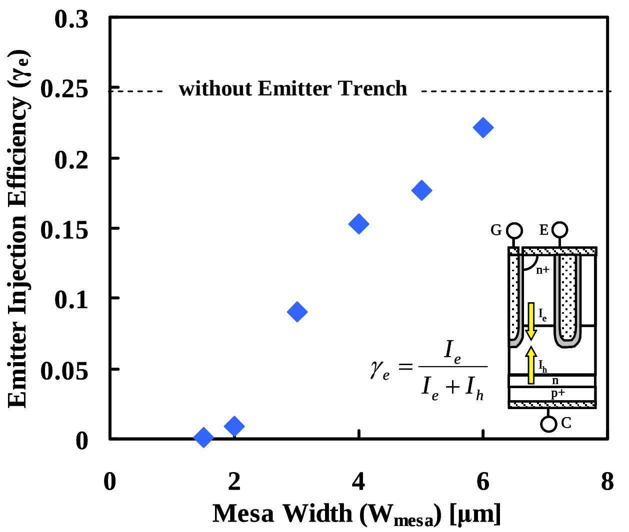

Fig. 5 Mesa width dependence of emitter injection efficiency.

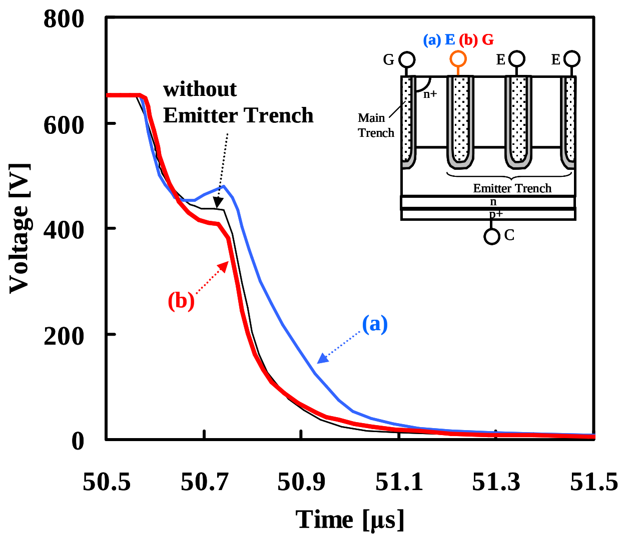

Fig. 6 Turn-on voltage waveforms with different structures.