Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp958-959

RF Characteristics of LDMOS Transistors with Superjunction Structures

Bo-Yuan Chen[1,2], Kun-Ming Chen[1], Guo-Wei Huang[1] and Edward-Yi Chang[2]

[1]National Nano Device Laboratories
No.26, Prosperity Rd. I, Science Park, Hsinchu 30078, Taiwan
Phone: +886-3-5726100 E-mail: bychen@narlabs.org.tw
[2]Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan

Abstract

The dc and RF characteristics of LDMOS transistors with superjunction (SJ) structures are investigated. To suppress the substrate-assisted depletion effect, tapered n- and p-pillar layouts in the SJ region are used. Experimental results show that the breakdown voltage and the cutoff frequency are enhanced by using the tapered SJ layout.

1. Introduction

Silicon laterally diffused metal-oxide-semiconductor (LDMOS) transistors are the mainstream technology for RF amplifiers in wireless communication systems or base-stations [1]. One of the main issues concerning the design of the LDMOS is the trade-off between the breakdown voltage capability and the on-resistance [2]. To solve this problem, the superjunction (SJ) concept was proposed by replacing the n-drift region of the LDMOS with a set of alternating n- and p-type pillars [3]. However, the majority of literatures focus on investigating the dc characteristics of SJ LDMOS, and its RF performances are less discussed. In this work, we demonstrate the dc and RF characteristics of SJ LDMOS. The tapered SJ structure, which can be implemented through conventional SJ device process without adding any extra mask, is adopted to suppress the substrate-assisted depletion effect [4].

2. Device Structure

The n-channel LDMOS transistors were fabricated using a 0.5-μm CMOS process with a gate oxide thickness of 125 Å. The channel length and the drift length are 0.8 and 3.4 μm, respectively. The LDMOS with a tapered SJ structure is shown in Fig. 1. Both the column widths of n- and p-pillars at the channel side are 0.8 μm. Because the width of the n-pillar is increased near the drain, excess carries in n-pillars compensate for the space charge induced by the p-substrate. Consequently, the substrate-assisted depletion effect can be suppressed. The devices under test have a multifinger gate configuration featuring 4 fingers with a total width of 160 μm for RF applications.

3. Results and Discussion

Fig. 2 shows the off-state breakdown voltage (V_{BD}) and the on-resistance (R_{ON}) of SJ LDMOS with different p-pillar widths at the drain side (W_t). The increased V_{BD} with decreasing W_t suggests the substrate-assisted depletion effect could be reduced efficiently by tapering the p-pillars near the drain [5]. Because the equivalent column width of the n-pillar is increased with decreasing W_t, the resistance in the drift region is reduced, leading to the reduction of R_{ON}. V_{BD} and R_{ON} are improved by 51% and 31%, respectively for devices with W_t=0.2 μm as compared to the conventional device (W_t=0.8 μm).

The output characteristics of SJ LDMOS are shown in Fig. 3. At high gate voltages, the tapered SJ device exhibits higher drain currents compared to the conventional SJ one, owing to the suppression of quasi-saturation effect. Moreover, we observe that the drain current in the conventional SJ device increases rapidly at high gate voltages when the drain voltage is higher than 20 V, which is caused by impact ionization in the drift region [6]. For tapered SJ devices, the rapid increase of drain currents is eliminated due to the smaller drift resistance.

Fig. 4 shows the cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) of SJ LDMOS at drain voltage V_{DS} = 20 V. As compared to the conventional SJ device, the enhancements of peak f_T and peak f_{max} are 32% and 54%, respectively, for the tapered device. When considering the drain resistance (R_d), f_T and f_{max} can be expressed as [7]

$$f_T \approx \frac{g_m}{2\pi\left[C_{gs} + C_{gd}\left(1 + g_m R_d\right)\right]} \quad (1)$$

$$f_{max} \approx \frac{f_T}{\sqrt{4 g_{ds} R_g + 8\pi f_T C_{gd}\left(R_g + (C_{gd}/C_{gg}) R_d\right)}} \quad (2)$$

where g_m is the transconductance, C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, g_{ds} is the channel conductance, and R_g is the gate resistance. We extracted the small-signal parameters from S-parameters to demonstrate the variations of f_T and f_{max} with different SJ structures. These parameters are listed in Table I. Higher f_T and f_{max} in the tapered device are mainly attributed to its lower R_d, since other parameters are less influenced by changing SJ layouts. Because the drift resistance of the tapered device is smaller than that of the conventional device, the tapered device exhibits a lower R_d. Fig. 5 summaries the breakdown voltage and the cutoff frequency of SJ LDMOS with different W_t. There is no trade-off between V_{BD} and f_T with decreasing W_t, and the highest V_{BD} and f_T are achieved for devices with a narrowest p-pillar width at the drain side (W_t = 0.2 μm).

4. Conclusions

The dc and RF characteristics of LDMOS transistors with SJ structures were presented. The devices with a tapered SJ layout exhibited better device performances compared with the conventional SJ ones. Higher breakdown voltages and cutoff frequencies were achieved by narrowing the p-pillar width at the drain side. The results suggest LDMOS transistors with a tapered SJ layout could be suitable for RF power applications.

Acknowledgements

This work is supported in part by the Ministry of Science and Technology, Taiwan under contracts MOST 103-2221-E-492-044, MOST 103-2221-E-492-052, and NCTU-UCB I-RiCE program under contracts MOST 104-2911-I-009-301.

References

[1] F. van Rijs *et al.*, *Int. Electron Device Meeting Tech. Dig.* (2006) 11.

[2] A. Parpia *et al.*, *IEEE Trans. Electron Devices* **37** (1990) 789.

[3] Sameh G. Nassif-Khalil *et al.*, *IEEE Trans. Electron Devices* **51** (2004) 1185.

[4] Wei Wu *et al.*, *IEEE ICSICT* (2012) 1.

[5] I. Y. Park *et al.*, *IEEE Circuits Devices Mag.* **22** (2006) 10.

[6] W. Yao *et al.*, *IEEE Trans. Electron Devices* **59** (2012) 1863.

[7] H. H. Hu *et al.*, *Jpn. J. Appl. Phys.* **46** (2007) 2032.

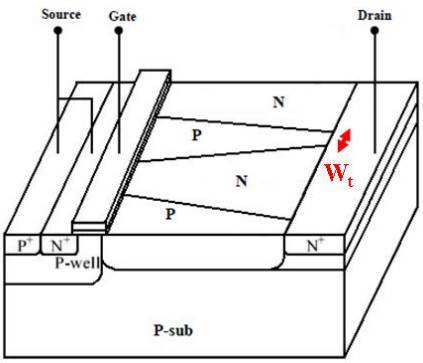

Fig. 1 Three-dimensional view of a SJ LDMOS used in this work.

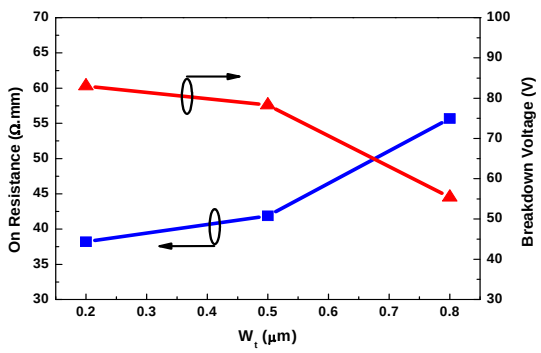

Fig. 2 Breakdown voltage (V_{BD}) and on-resistance (R_{ON}) of SJ LDMOS with different p-pillar widths at the drain side (W_t).

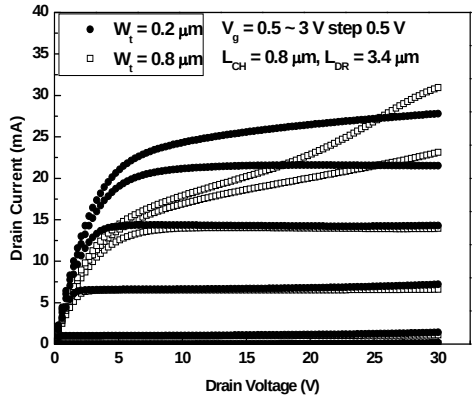

Fig. 3 Output characteristics of SJ LDMOS transistors with different W_t.

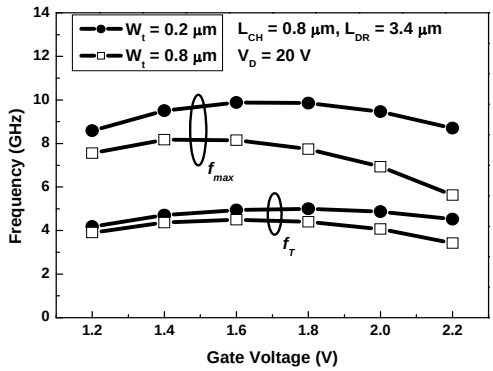

Fig. 4 Cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) of SJ LDMOS with different W_t.

Table I Extracted small signal parameters of SJ LDMOS with different W_t at V_{GS}=1.6 V and V_{DS}=20 V.

	R_d (Ω)	R_s (Ω)	R_g (Ω)	g_m (mS)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	g_{ds} (mS)
W_t=0.2μm	99	7.9	3.7	14.9	442	75	192	1.14
W_t=0.8μm	148	7.4	4.1	14.8	461	76	193	1.10

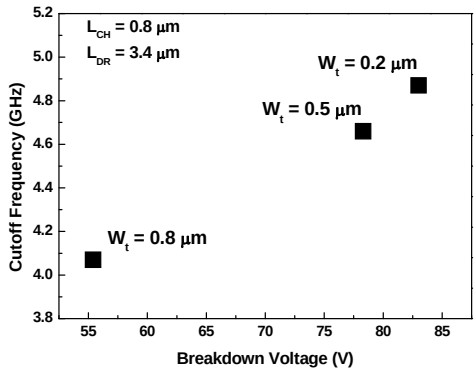

Fig. 5 Breakdown voltage and cutoff frequency of SJ LDMOS with different W_t.