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4H-SiC Vertical Gate Trench with a Well-Controlled Shape Uniformly Formed by High Rate Etching and Annealing with Solid Source

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Abstract

This article describes a novel trench forming process to develop silicon carbide implantation and epitaxial trench metal-oxide-semiconductor field-effect transistors (SiC-IETMOSFETs). Well-controlled trench structures with vertical trenches (approximately 88 degrees) and without the sub-trenches were fabricated by dry etching with sub-trench suppress films deposited simultaneously. Moreover, high trench etching rate (above 500 nm/min) and excellent etching rate uniformity of ±1.5% were achieved. The annealing with solid-source SiC producing quasi thermal equilibrium conditions was optimized to remove dry etching damage on the trench sidewalls and form round corners of trench top for gate oxide coverage. The applicability of the trench forming process has been successfully demonstrated by the fabrication of IETMOSFETs with 0.6-1.1 µm trench widths.

1. Introduction

Applications using SiC-MOSFETs have been expected to greatly reduce the electrical energy consumption due to low on-resistance [1]. In order to improve high channel resistance, Harada *et al*. have developed IEMOSFETs, whose p-base region and channel are formed by ion implantation and epitaxial layer, respectively [2]. A trench SiC-MOSFET has been expected to have low specific on-resistance because of its high cell density and high channel mobility on the trench sidewall [3]. The authors have developed IETMOSFET [4]. However, it remains an important challenge to improve trench forming processes. The electric field concentration at the sub-trenches is considered to cause breakdown at low voltage [5]. The damage and roughness on the trench sidewall affect the lifetime of the gate oxides [6]. In this study, the authors optimized the process of trench forming by high rate etching and annealing with solid source, and demonstrated IETMOSFETs.

2. Experimental

SiC trenches were fabricated on n-type and 4˚ off-axis 4H-SiC substrate of 76 mm diameter. Line and space mask patterns were fabricated on the wafer deposited with a SiO_2 film of 1 µm thickness. The trenches formed by inductively coupled plasma reactive ion etching (ICP-RIE) were annealed with solid-source SiC after removing SiO_2 mask. Annealing conditions were conducted at 1.2×10^4 Pa for 18 min and varied from 1350˚C to 1605˚C. Curvature radius, width and depth of the trenches were measured by a scanning electron microscope (SEM). IETMOSFETs with 0.6-1.1 µm trench widths at the same cell pitch of 10.6 µm were fabricated with these trench forming processes. The other detailed fabrication processes and I-V measurements will be reported elsewhere [4].

3. Results and Discussion

Figures 1 show SEM images of typical SiC trench shapes. The trench with vertical sidewalls was formed by the dry etching, whose angle was approximately 88 degrees. Kutsuki *et al*. reported that as the trench angle approaches 90 degrees, the SiO_2/SiC interface state density decreases and the effective channel mobility increases [7]. Sub-trenches were not formed at the bottom of the trenches. The desired trench shape was successfully formed.

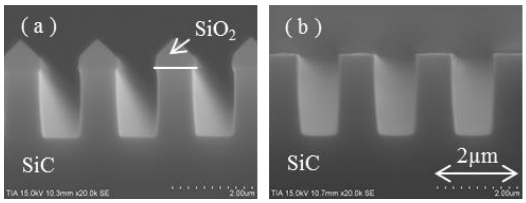

Fig. 1 Cross-sectional SEM images of typical SiC trenches: (a) with SiO_2 mask, (b) without SiO_2 mask (before annealing)

Mechanism to suppress sub-trenches is shown in Fig. 2. Reaction of etching gas and passivation gas produces thin films which are deposited at the edge of the trench top and on the sidewalls of the trench. The width of the trench top is narrowed. The film causes to suppress etching of the trench bottom edge.

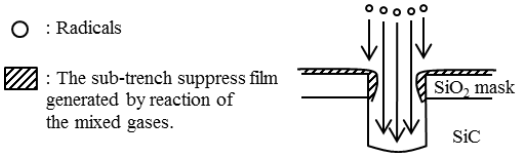

Fig. 2 Schematic of mechanism to suppress sub-trenches.

In order to investigate productivity for trench fabrication, depth and width of the trenches within wafer were measured. In the Fig. 3, open circles indicate uniformity of SiC trench etching rate and filled circles indicate the width of

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the trench top normalized by the bottom space width of SiO_2 mask. Excellent etching rate uniformity of ±1.5% was achieved at high etching rate (above 500 nm/min). The uniformity of the dimension ratio was ±2.2%.

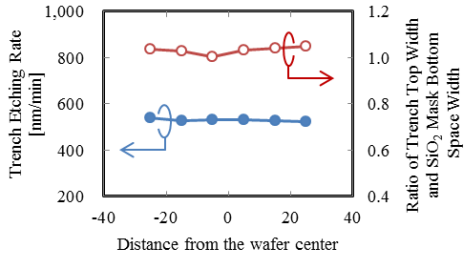

Fig. 3 Wafer uniformity of SiC trench etching rate (filled circles) and dimension ratio of trench top width (open circles).

Dry etching damage to the sidewalls of the trench should be caused. It was reported that trench sidewalls were improved using chemical dry etching [6]. Trenches after removing SiO_2 mask formed by the dry etching were annealed in hydrogen ambient with the solid-source SiC, which produces quasi thermal equilibrium conditions to minimize the Si desorption from the samples. Figures 4 show SEM images of annealed trenches. The trenches annealed at 1350˚C and 1400˚C were not etched. The width of trenches before and after annealing at 1500˚C was slightly enlarged to approximately 40 nm. When annealing at 1500˚C and 1605˚C, the curvature radii of the trench top corners were approximately 150 nm and 360 nm, respectively. Suitable round corners of trench top are necessary for uniform coverage of gate oxide and should be controlled to contact the implanted source region to the epitaxial channel.

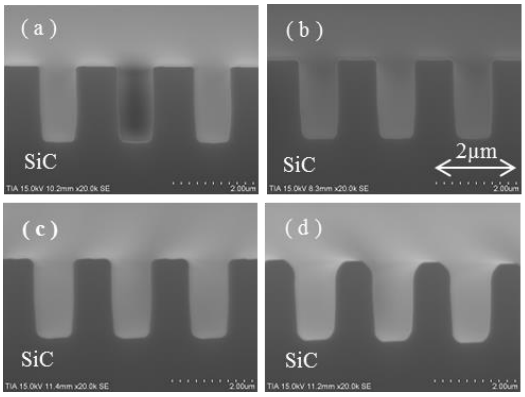

Fig. 4 Cross-sectional SEM images of SiC trenches annealed with solid source: (a) 1350˚C, (b) 1400˚C, (c) 1500˚C, (d) 1605˚C.

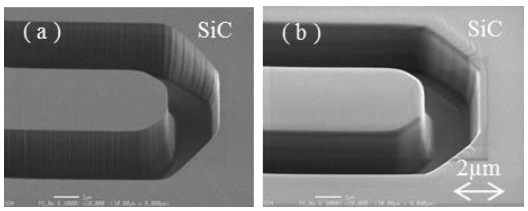

Fig. 5 SEM images of SiC trench before (a) and after (b) the annealing with solid source at 1500˚C for reducing surface roughness of the trench sidewalls.

Roughness on the sidewalls of the trench was reduced by the annealing with solid source at 1500 ˚C, as shown in Fig. 5. Smooth surface on the trench sidewalls enhances gate oxide reliability [6].

Figure 6 shows trench width dependence on blocking voltage and specific on-resistance at the same cell pitch. The IETMOSFETs with 0.6-1.1 μm trench widths were demonstrated with the trench forming process.

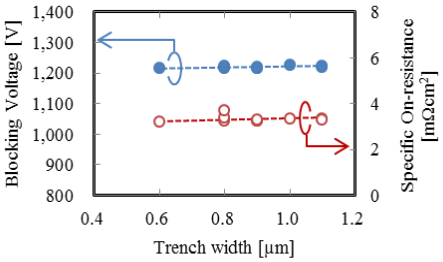

Fig. 6 Trench width dependence on blocking voltage (filled circles) and specific on-resistance (open circles).

4. Conclusions

The Trench forming processes with high rate etching and annealing with solid source were optimized. The desired trench shape with approximately 88 degrees trench angle and without the sub-trench was formed by the dry etching. High etching rate of above 500 nm/min and the excellent etching rate uniformity of ±1.5% were achieved. When annealing at 1500˚C, the trench width was enlarged to approximately 40 nm to remove damage layer and the curvature radius of the trench top corner was approximately 150 nm. The IETMOSFETs with 0.6-1.1 μm trench widths have been successfully demonstrated, which shows the potential of further reduction of the cell pitch for lower on-resistance.

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