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Threshold-Voltage Instability in SiC MOSFETs

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Abstract

This work reports on three important aspects of threshold-voltage instability in SiC power MOSFETs: (1) the threshold-voltage instability observed in commercial devices, (2) the basic mechanisms driving this instability, and (3) the need for improved test methods when qualifying devices.

1. Introduction

Instability of the threshold-voltage (V_T) in SiC MOSFETs, first reported at the 2005 ICSCRM [1], has become an important reliability issue in the past few years. As such, it has been studied by a number of different research groups in recent years [2-14]. This work reports on three important aspects of the issue: (1) the V_T instability observed in commercial devices, (2) the basic mechanisms driving this instability, and (3) the need for improved test methods when qualifying devices.

It has generally been observed that a negative gate-bias stress causes a negative shift of V_T and a positive bias stress causes a positive shift. If V_T shifts negatively too much for these n-channel devices, it can lead to significant leakage current in the off state, potentially resulting in catastrophic device failure. On the other hand, too large a positive shift in V_T may result in increased on-state resistance, reducing device efficiency. Results reported at the 2014 ECSCRM conference showed that some commercial devices experienced significant V_T shifts during bias temperature stress, under both negative and positive bias [15]. It has been subsequently reported that significant improvements in V_T stability have been observed in the most recently available commercial devices [16].

2. Discussion

There are two basic mechanisms that affect the V_T stability: oxide-trap activation and oxide-trap charging [2]. The oxide traps themselves are defects related to an oxygen vacancy, resulting in a weak Si-Si bond. If this bond is broken, the defect becomes an active trap site, referred to in some of the literature as an E′ center [17]. Once active, it may then engage in charge trapping. In fact, the E′ center is known to be a hole trap. Trapped positive charge in the gate oxide results in a negative shift in V_T. But under positive gate-bias, electrons from the SiC substrate may tunnel into the oxide and form a charge-neutral dipole [2, 17, 18], causing a positive shift in V_T. If a negative bias is then applied, electrons may tunnel back out of the oxide, uncovering the positive trapped charge and causing V_T to shift negatively once more. At room temperature, this effect is repeatable. For some devices, especially those of earlier vintage, this V_T instability increases considerably during a bias temperature stress at temperatures at and above 150 °C. This increase in V_T instability, whether determined by a unipolar gate-bias stress or a back-and-forth bipolar stress-and-measure sequence, is likely due to the activation of additional E′ centers in the oxide [2, 19], with an activation energy of about 1.1 eV [2].

When activation is not present, the V_T shift generally exhibits a linear-with-log-time response to a bias stress. This is because the oxide-trap charging occurs via a direct tunneling mechanism [17, 18]. In fact, a two-way tunneling model predicts a tunneling front that proceeds from the interface into the oxide at a rate of 1.5 to 2 Å per decade of time [20]. This implies that the oxide traps close to the interface can change charge state very, very quickly, and suggests that the time taken to measure the effect of a stress greatly affects what is observed. If there is too long a delay following the removal of the stress bias, or the bias applied during the measurement is present for an extended period of time, then the full effect of the bias stress will not be observed [2].

Present test methods employed by industry qualification standards (Automotive Electronics Council Q101 [21]—based on the JEDEC JESD-22 A108C test method [22]) and military standards (MIL-STD-750 [23]—test method 1042.3 for device burn-in and life-testing) allow long delay times such that devices that would have been deemed to have failed by shifting too much may instead be judged to be stable [24]. Thus, improved test methods are needed [25].

Processing also affects V_T stability. Since some V_T instability is observed in as-processed devices at room temperature prior to bias-temperature stressing, clearly some trap activation must occur during processing. Furthermore, it has been previously reported that the standard nitrogen-based post-oxidation anneal, used to suppress interface traps and improve channel mobility, also reduces V_T instability [18, 26]. Other recent results indicate the benefits of a P-based anneal as well [27].

3. Conclusions

Threshold-voltage instability has proven to be an important reliability issue in SiC power MOSFETs in recent years. Very recent results by some commercial vendors show very dramatic improvements in the stability of this

threshold voltage. Improved reliability test methods would increase confidence that generally good devices have been successfully distinguished from bad devices.

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