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Design of Complementary Raised-Drain Tunneling FET for Ultra-Low Voltage Applications

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Abstract- A new architecture of raised-drain FETs with face tunneling has been proposed to improve the device performance. Moreover, for the first time, the body effect of TFETs has been studied by using a body-contacted GeOI wafer. With a forward body bias, TFET shows higher I_{on} with the penalty of larger I_{off}. Demonstrated on SRAM cell as a benchmark, this newly designed TFET with a body-bias can be successfully operated down to V_{dd}= 0.2V and shows much better noise-margin in comparison to conventional CMOS SRAM. These results show good potentials of the new structure for ultra low voltage applications.

1. Introduction

As we approach the scaling limit of planar CMOS, we have strong demand in the portable and wearable products for wireless communications. It is urgently needed to design high performance but with very low voltage and low power devices. But the sub-threshold swing (S.S) of CMOS devices can never cross the boundary of 60mV/decade and limits the operation voltage (V_{dd}). Therefore, super steep S.S. devices emerged as a possible candidate [1,2], and one of them, Tunneling FET (TFET)[3], becomes a major player because its S.S. can be smaller than 60mV/decades owing to its nature of Zener bad-to-band tunneling (B2BT). It allows V_{dd} to be scaled. To further improve TFET performance, increasing the tunnel region of the hetero junction by a mismatched bandgap is a better solution [4]. However, the increase of the tunnel region beneath the gate tends to limit the distance between source and drain, which then limits the scalability. On the other hand, another critical issue, i.e., unexpected large gate-to-drain capacitance, C_{gd}, which is crucial to the delay of logic circuits, has seldom been discussed [5]. In this paper, we will provide a solution of complementary-TFET (CTFET) with a good scalability and a much lower C_{gd}. Furthermore, we will also study the body effect of CTFETs on GeOI wafer. Finally, a benchmark will be carried out on an SRAM cell to demonstrate its capability for ultra low voltage applications.

2. Device Description

Fig. 1 lists 3 different device structures and their pros and cons. Fig. 1a is a conventional TFET with edge-tunneling, 1b has a face-tunneling region to improve the Ion current. To solve the Cgd issue, a new structure, Fig. 1c, using raised-drain may greatly increase the Ion current by a reduction of Cgd. The E.O.T. of these devices is 1nm, composed of HK dielectrics. Fig. 2 is the process flow to prepare the devices on a body-contacted GeOI, following by selective epitaxy of hetero-materials respectively on Si and Ge.

3. Results and Discussion

A. Design of Face Tunneling FET with a Raised-Drain

Since tunnel current is proportional to the tunnel area, instead of the conventional source-edge tunnel FET, face tunnel FET (Fig. 1b) was proposed by extending the source deeply into the channel to form a large tunnel region between the extended source and gate. However, the more source extension into the channel, the shorter the distance between source and drain (L_{sd}) becomes. It induces the leakage, degrades S.S., and thus worsens the short channel effect. Therefore, we proposed a new structure by eliminating the source-to-drain leakage by inserting i-layer between the source and drain, in Fig. 1(c), and releases the constraint of L_{sd}. Figs. 3&4 compare I_dV_{gs} and S.S. for three device structures in Fig. 1 respectively. Face TFET w/raised-D shows steeper S.S. as a result of a reduction of source-to-drain leakage and the highest I_{on} current achieved because of an extra tunnel region. Fig. 5 shows that the device w/raised-D kept good S.S. as L_{sd} scales down to 10nm. This is explained in Fig. 6, in which the raised-D one forms a channel barrier at off-state to prevent the leakage; however, the channel barrier of the one w/o raised-D is pulled down by the drain, yielding the leakage. As a whole, raised-D TFET received 200% I_{on} enhancement and 28mV/decade S.S., shown in Fig. 7.

B. Study of C_{gd} and Body Effect for TFETs on GeOI

In CMOS devices, C_{gd} is just half of C_{inv}, while in conventional CTFET, the value is 90% of C_{inv}, which is the origin of circuit delay, Fig. 8. However, in TFET with raised-drain, it exhibits a smaller delay, since in the strong inversion, a channel barrier built in the raised-D device weakens the capacitance coupling effect, Fig. 9. Moreover, a body contact offers the advantage of excellent electrostatic through the buried oxide. Figs. 10&11 show I_dV_{gs} of the raised-D TFETs modulated by the body bias. When a forward body bias is applied, I_{on} is enhanced but with the penalty of I_{off} increment; if a reversed body bias is applied, I_{on} is reduced instead. One can strengthen or weaken the devices by body biases. Furthermore, the body effect of TFETs is very sensitive to thickness of Ge body. The thinner the body is, the stronger the effect is, Fig. 12. Finally, I_dV_{gs} of TFETs is superior to that of CMOS devices with low operation power (LOP) and comparable to that of high performance (HP), Fig. 13.

C. Benchmarks of *Body-contacted CTFET SRAM*

Since CTFET is a one-direction device, bi-directional pass-gate, composed of two paralleled and reversed nTFETs, are designed to serve as pass-gate in 8T CTFET SRAM with additionally body terminals, Fig. 14. In order to take the advantage of body-bias, the pull-down gates are applied by a forward body as read; the access gates are assisted by a forward body as write, Fig. 15. If without a body bias, the butterfly curves show CTFET SRAM with larger noise margin at low V_{dd}, compared to that of CMOS one, Fig. 16. If body biases are used, the read noise margin (RNM) and write noise margin (WNM) of CTFET SRAM show further improvement, Figs. 17&18.

In summary, a new structure of Tunneling FET with a raised drain has been proved by simulation and demonstrated a steeper S.S and higher Ion. This is the result of a low C_{gd}, and the reduction of source-to-drain leakage. Moreover, the body effect has been studied and employed to provide good performance of SRAM. WUsing forward body bias during read and write, RNM and WNM show further improvement, and the SRAM can be successfully operated with V_{dd} down to 0.2V with good noise margin. These results will be very helpful to design the ultra-low voltage circuit based on this new CTFET.

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References: [1] C. Onal et al., EDL, vol. 30, p. 64 (2009). [2] A. Padilla et al., IEDM, p. 171, 2008. [3] Y. Morita et al., EDL, p. 792, 2014.[4] W. Wang et al., EDL, p. 193, 2014. [5] H. Liu et al., DRC, p. 233, 2012.

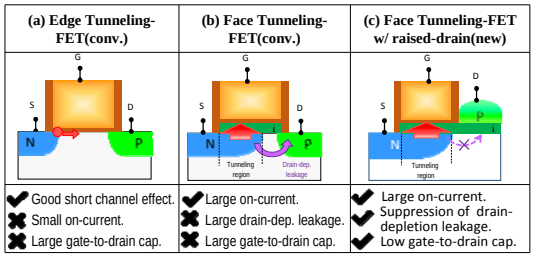

Fig. 1 Three kinds of heterojunction TFETs are compared in this work, i.e., edge tunneling FET, face tunneling FET, and the face tunneling FET with raised-drain.

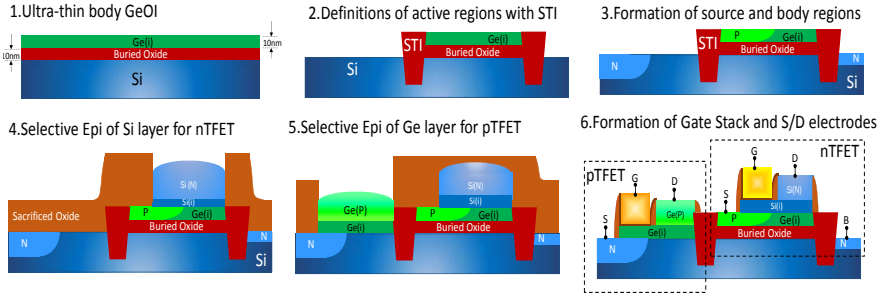

Fig. 2 The process flow of the complementary raised-drain TFET by using GeOI wafer, which constructs the hetero-junction by selective epitaxial growing material on Si substrate and Ge thin body respectively to implement the hetero p-i-n tunneling junction between the source and drain.

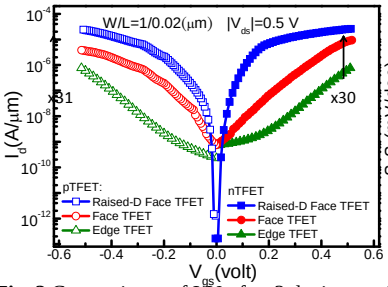

Fig. 3 Comparisons of I_d-V_{gs} for 3 device structures in **Fig. 1**, which shows the raised-D one obviously reduces the sub-threshold leakage and greatly enhances I_{on}.

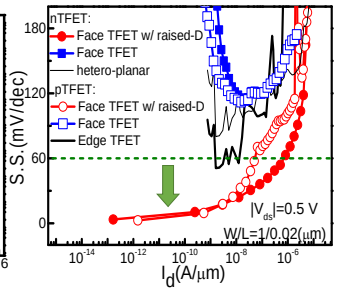

Fig. 4 Since the leakage of the raised D has been suppressed, the S.S. shows dramatic improvement, compared to the other two cases.

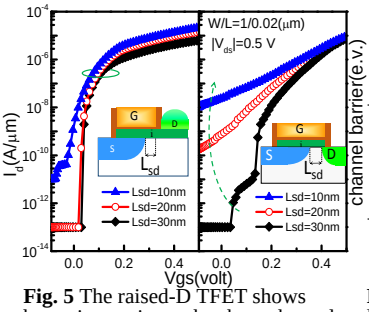

Fig. 5 The raised-D TFET shows better immunity to the short-channel effect as the space between drain and source are scaled, compared to the other split.

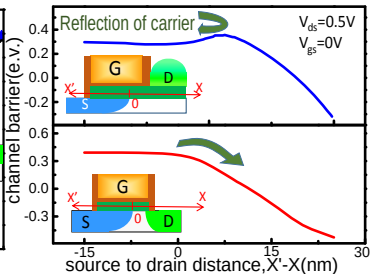

Fig. 6 Since there is an intrinsic doped layer sandwiched between source and drain in raised-D TFET(upper one), the electric field cannot directly penetrate both terminals to form a leakage path.

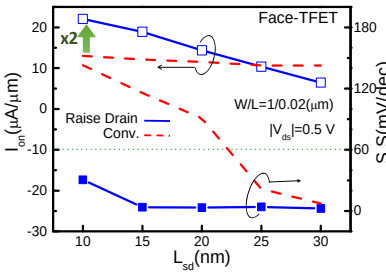

Fig. 7 By adjusting the space between source and drain, L_{sd}, one can optimize the characteristics of raised-D TFET in terms of I_{on} and S.S., and L_{sd} can be shrunk to less than 10nm.

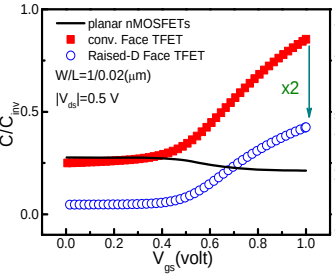

Fig. 8 The gate-to-drain capacitance, C_{gd}, is also decreased in the new structure, in comparison to that of conventional face TFET, which will further reduce the delay time.

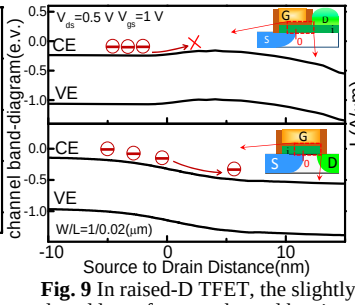

Fig. 9 In raised-D TFET, the slightly-doped layer forms a channel barrier to alleviate the coupling-ratio of inversion carriers from the gate to drain (*top*), which effectively reduces the C_{gd}.

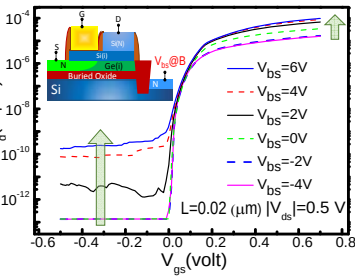

Fig. 10 The 10nm buried oxide layer on GeOI facilitates additional body terminal to modulate the tunneling current characteristics, enlarged by a forward body-bias, and reduced by a reversed bias.

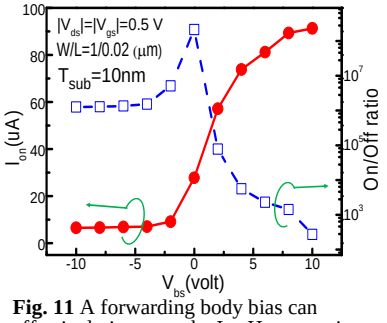

Fig. 11 A forwarding body bias can effectively improve the I_{on}. However, it comes along with huge leakage increase. On the other hand, a reversed body bias might slightly decrease I_{on}.

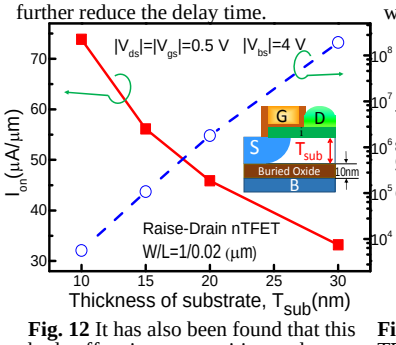

Fig. 12 It has also been found that this body effect is very sensitive to the substrate thickness, T_{sub} of Ge body in GeOI. One can narrow T_{sub} to decrease the body bias.

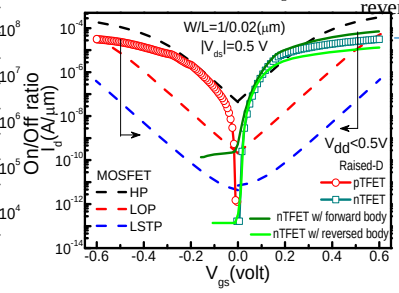

Fig. 13 Comparisons between the raised-D TFET and 20nm CMOS devices, which shows that this device beat LOP and LSTP CMOS device at V_{dd}=0.5V

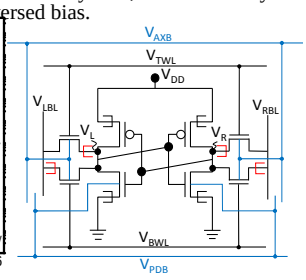

Fig. 14 A body-biased 8T CTFET SRAM cell performance has been proposed and evaluated.

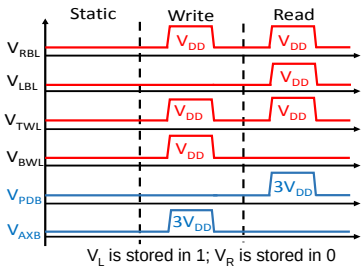

Fig. 15 The operation scheme of 8T CTFET SRAM. The write is assisted by the body bias from pass gates; the read is assisted by the body bias from the pull-down gates.

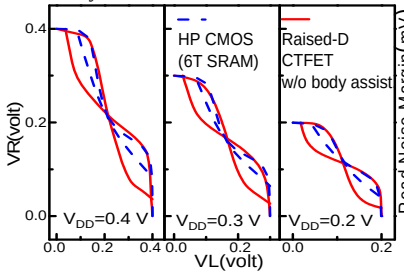

Fig. 16 The butterfly curves during read show that the CTFET SRAM can be operated down to 0.2V and is superior to HP CMOS SRAM at such low operation voltages.

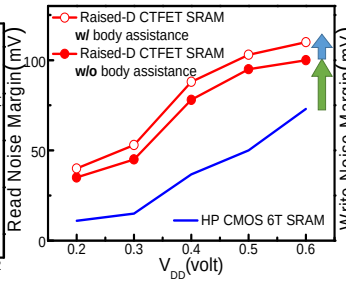

Fig. 17 By applying forward body bias on the pull-down gates, the RNM is further improved, compared to that without the body-

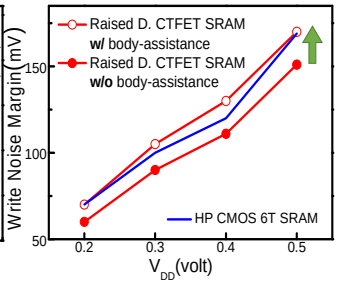

Fig. 18 By applying a forward body bias on pull-down gates during writing, the WNM of CTFET SRAM can overtake that of HP CMOS SRAM.