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Steep Subthreshold Swing Metal-Oxide-Semiconductor Field-Effect Transistors Utilizing Nonlinear Gate Dielectric Insulators

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Abstract

We propose nonlinear-dielectric metal-oxide-semiconductor electric-field transistors (NLD-MOSFETs), which utilize the nonlinear dielectric material as the gate insulator to realize near-threshold-voltage operation. TCAD simulation reveals that combination of the electrostatics in the depletion mode and nonlinearity of the gate permittivity can lead to excellent sub-thermal subthreshold swings (34 mV/decade) with high I_{on} comparable to those of the conventional MOSFETs.

1. Introduction

The steep slope transistor, which surmounts the physical lower limitation of the subthreshold swings (60 mV/decade at 300K) in the conventional MOSFETs has attracted rising attention because of a potential workhorse for energy efficient logic device for future VLSI technology [1]. Although the tunneling FETs (TFET) have been extensively studied [2-5] as a candidate of the steep slope devices, the relatively lower I_{on} than those of the conventional MOSFETs due to the tunneling barrier is a technology hurdle for integration. Recently, as the negative capacitance effects in the ferroelectric gate MOSFETs [6-8] have stirred a strong interest as another solution for simultaneous implementation of both higher I_{on} and sub-thermal subthreshold swing, engineering to stabilize and exploit such the quasi-stable states is still elusive. In this paper, we propose nonlinear dielectric metal-oxide-semiconductor electric-field transistors (NLD-MOSFETs) to ensure both a sufficient I_{on} and sub-thermal switching based on TCAD simulation.

2. Device Structure and TCAD Simulation

Device structure

Figure 1 illustrates a schematic of the proposed NLD-MOSFETs. In NLD-MOSFETs, the operation of the depletion mode is a key for a steep switching. In our TCAD simulation, the silicon-on-insulator (SOI) structure was adopted as the channel. The body thickness was 10 nm. The gate stack was comprised of the 5-nm-thick non-linear dielectric gate insulator and the gate electrode with the work-function of 5.1 eV (a valence band edge metal). The dopant concentrations in the source, the drain and the channel regions were 1×10^{20}, 1×10^{20}, and 5×10^{18} cm^{-3}, respectively. The dopant type of those regions were n-type.

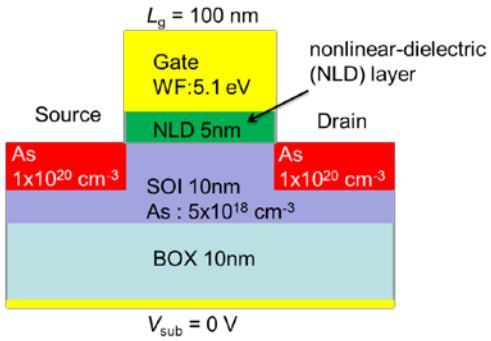

Fig. 1 A schematic diagram of NLD-MOSFETs

Framework of TCAD simulation

As a dependence of the dielectric constant of the gate insulator on the electric field, we assumed a Gaussian curvature of

$$\varepsilon(E) = \varepsilon_{r0} + A\exp[-(E-E_c)^2/E_{width}^2] \quad (1).$$

This dependency is found widely in high dielectric materials or ferroelectric materials such as (Sr, Ba)TiO_3 [9], where ε_{ro}, E, E_c, and E_{width} are the dielectric constant of the field independent component, E is the electric field, E_c is the electric field at the maximum dielectric constant, E_{width} is a parameter which indicates the sensitiveness of the permittivity to E as seen in Fig. 2(a).

The tool we used in TCAD simulation was Hy-

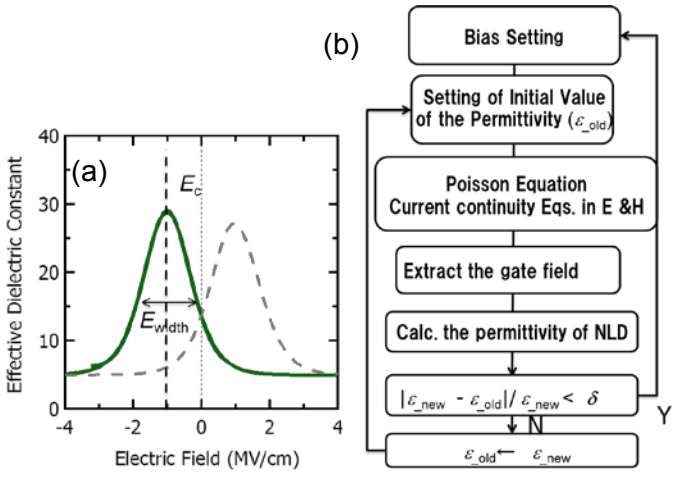

Fig. 2 A modeling of the dielectric constant of the gate insulator. Gaussian curvatures shown in (a) were assumed. (b) The self-consistent calculation procedure using an iterative method.

ENEXSS^{TM} [10]. As shown in the diagram of Fig. 2(b), the nonlinear gate dielectric function in eq. (1), the Poisson equations and the continuity equations in the device were self-consistently calculated via an iterative computation.

3. Results and Discussion

Figure 3 shows the gate transfer curves for NLD-MOSFETs (the solid curves). In this simulation, we assume E_c = 1.2 MV/cm so as to change steeply the permittivity in the subthrehold region (Fig. 4). The sub-thermal SS of less than 40 mV/decade is attained in NLD-MOSFETs. To understand intuitively the working principle of the devices, those for conventional depletion type MOSFETs with constant permittivity gate dielectrics are superimposed in Fig. 3 as a parameter of the permittivity (the dashed curves). In the conventional MOSFETs, the transfer characteristics such as the threshold voltage are sensitive to the electrostatics in the gate (the equivalent oxide thickness), especially in the depletion mode. Therefore a sharper descend of the nonlinear dielectric constant in NLD-MOSFETs results in the steeper SSs shown in Fig. 3. It is notable that a comparable amount of I_{on} is possible in NLD-MOSFETs.

To elucidate a link of the nonlinearity in the gate dielectric constant and the surface potential ψ_s, the potential distributions along the center of the device are plotted in Fig. 5(a) as a parameter of the gate voltage V_G. Moreover, $dV_G/d\psi_s$ in the device center as a function of V_G is also depicted in Fig. 5(b). As seen in Fig. 5(a), the kinks which can be seen in in the potential curves at the interface of NLD/SOI indicate differences in the permittivity between SOI and the NLD layer. The gradual variation of the degree in the kinks means that the Poisson equation and the nonlinear dielectric function shown in eq. (1) were solved self-consistently.

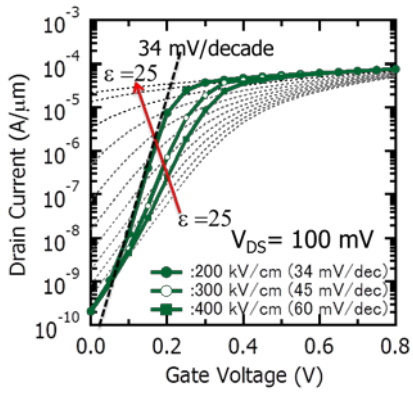

Fig. 3 The transfer curves for NLD-MOSFETs (the solid curves). Those for the MOSFETs with constant permittivities (the dashed curves) are superimposed.

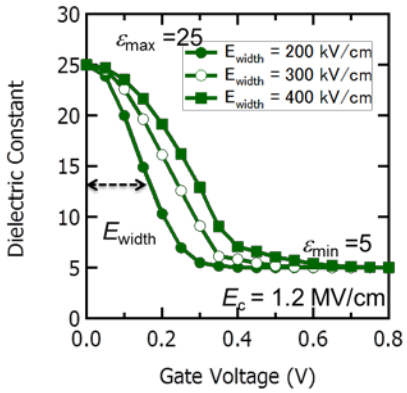

Fig. 4 The permittivity of the NLD layer versus the gate voltage as a parameter of E_{width}.

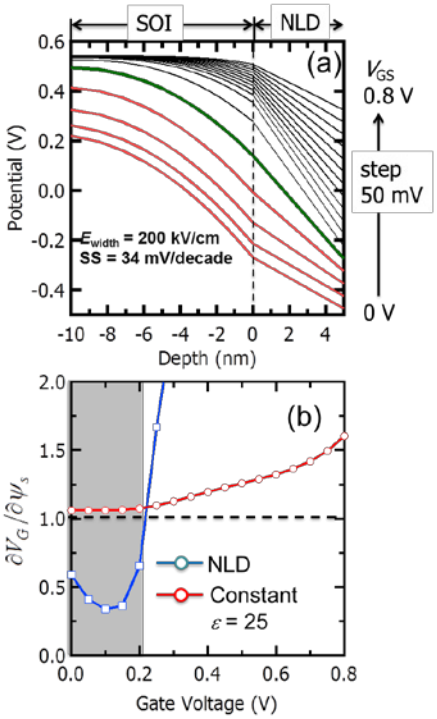

Fig. 5 The Potential distributions of NLD-MOSFET in the center of the gate stack (a). $\partial V_G/\partial\psi_s$ for NLD-MOSFETs and those for MOSFETs with the gate of $\varepsilon = 25$.

Looking at the $\partial V_G/\partial\psi_s$ extracted from Fig. 5, it is evident that the nonlinear variation of the gate permittivity in conjunction with changing the gate voltage leads to the states of $\partial V_G/\partial\psi_s < 1$ in the subthreshold region and the sub-thermal switching. This result indicates NLD-MOSFETs are promising for the future logic device in the near-threshold-voltage operation regime.

4. Conclusions

A novel MOSFET (NLD-MOSFET), which embed the nonlinear dielectric material as the gate insulator have been proposed and its performances were investigated. Steeper SS less than 40 mV/decade and a high I_{on} comparable to conventional MOSFETs imply that the proposed device is an option for the logic device in the ultralow voltage applications.

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