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Variation Analysis for Ultra-Low Voltage 8T Tunnel FET SRAM Using Closed-Form Analytical Model of Static Noise Margin

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Abstract

Variations of 8T tunnel FET (TFET) SRAM cells at ultra-low supply voltage (V_{DD}) of 0.3V are discussed. A closed-form analytical model for static noise margin (SNM) of the TFET SRAM cell is proposed to clarify the dependence of SNM on device parameters, and is verified with the simulations. In addition, feasibility of the TFET SRAM cells operating at V_{DD}=0.3V in two different process technologies is evaluated using the proposed model.

1. Introduction

Reducing the supply voltage (V_{DD}) is a promising method to realize energy-efficient SRAM. Fig. 1 shows the energy dependence on V_{DD} for tunnel FET (TFET) and MOSFET SRAMs [1]. By using TFETs, further V_{DD} scaling down to around 0.3V effectively suppresses the energy thanks to steeper subthreshold swing (SS). Although there are several researches on such ultra-low V_{DD} TFET SRAM design [2,3], it is not clear how device parameters affects the SRAM cell stability. In this work, a closed-form analytical model for static noise margin (SNM) of a TFET SRAM cell is proposed for the first time to clarify the dependence of SNM on device parameters. Using the model, impacts of process variations in TFET SRAM design are analyzed.

All the simulations in this paper are conducted using the physics-based TFET compact model implemented as a Verilog-A model [4]. Fig. 2 shows the device structure. In this work, Ge-based TFETs are used [5] and I_{DS}-V_{GS} characteristics are shown in Fig. 3.

2. Proposed analytical model for SNM of TFET SRAM

In this paper, an 8T SRAM cell [2] shown in Fig. 4 is discussed, because it is difficult to use a 6T cell, which is widely-used in the MOSFET-based SRAM cells, due to the unidirectional characteristic of TFETs [3]. Fig. 5 shows the simulated butterfly curves of the 8T SRAM cell. In this paper, we focus on the read operation.

To calculate SNM analytically, two types of approximate equations are introduced based on the expressions for the subthreshold I-V characteristics of MOSFETs. First one is an approximate equation at around V_{DD} (Eq. (1) in Fig. 6). Second one is an approximate equation at around half V_{DD} (Eq. (2) in Fig. 6). These approximate characteristics are plotted as lines in Fig. 3. Using these equations (1) and (2), a closed-form expression of SNM can be derived as Eq. (3) in Fig. 6. The calculated SNMs by Eq. (3) are shown as dotted rectangles in Fig. 5. The standard deviation (σ) of the SNM variation can be derived from Eq. (3) and is given by Eq. (4) in Fig. 6 assuming that V_{TH} variations are dominant.

To verify the validity of the proposed analytical model, the model is compared with the simulations. Fig. 7 illustrates the cumulative probabilities of the SNM variation obtained by the simulations and Eqs. (3) and (4). Here, it is assumed that the within-die V_{TH} variations with the identical σ's in all the transistors of the 8T cell (denoted by σ_{VT}) are considered and they obey Gaussian distribution for simplicity. However, it should be noted that the proposed model (3) and (4) is valid no matter what distribution the V_{TH} variation follows. Fig. 8 shows the means (μ) and σ's of the SNM variations. The errors between the simulations and the proposed model are less than 2% for μ and 10% for σ when V_{DD} is 0.25-0.4V. This indicates that the proposed analytical model (3) and (4) is a good approximation for SNM of the 8T TFET SRAM cell.

Finally, a requirement for the V_{TH} variation in TFET SRAM design is discussed. The read failure probability (P_{RF}) of SRAM cells is given by Eq. (5) in Fig. 6. $\sigma_{VT,max}$ is defined as the maximum σ_{VT} to satisfy the condition that P_{RF} is less than 10^{-6}, which means that 1M bit SRAM cells can operate. Fig. 9 shows $\sigma_{VT,max}$ at V_{DD}=0.3V as a function of SS. This figure indicates that the V_{TH} variation must be reduced as SS becomes steeper to realize better energy efficiency.

3. Variation analysis in different process technologies

In this section, the following two process technologies; "state-of-the-art process" (L=20nm) and "cost-effective process" (L=65nm) are assumed, and the 8T TFET SRAM cells in those processes are discussed. The device parameters are summarized in Table I. The sources of variation are listed in Table II. Fig. 10 illustrates how those variation sources affect V_{TH} variation. This figure indicates that the work function (WF) variation is a major source of the V_{TH} variation and its influence becomes larger as device miniaturization advances. Fig. 11 shows P_{RF} obtained by the simulations and Eq. (5) in Fig. 6. The calculated P_{RF} agrees with that obtained by the simulations. P_{RF} of the SRAM cells in the state-of-the-art process increases significantly due to the large V_{TH} variation caused by the WF variation, while in the cost-effective process, P_{RF} at V_{DD}=0.3V is less than 10^{-6}, which means that 1M bit SRAM cells can operate at V_{DD}=0.3V.

4. Conclusions

Analytical model for SNM of the 8T TFET SRAM cell was proposed and verified with the simulations. Using this model, feasibility of 0.3V operation was discussed.

Acknowledgements This work was supported in part by NEDO.

References [1] H. Fuketa, et al., IEDM (2011) 559. [2] V. Saripalli, et al., NANOARCH (2011) 45. [3] X. Yang and K. Mohanram, DATE (2011) 1. [4] K. Fukuda, et al., JAP **114** (2013) 144512. [5] H. Fuketa, et al., JJAP **54** (2015) 04DC04. [6] ITRS, http://www.itrs.net [7] T. Matsukawa, et al., IEDM (2014) 300.

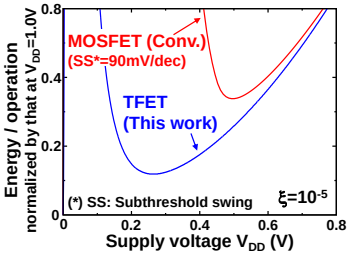


Fig. 1. Energies of TFET and MOSFET SRAMs. They are calculated by the energy model proposed in [1]. ξ is effective time ratio [1].

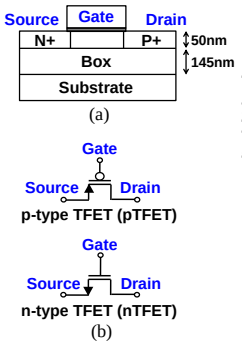
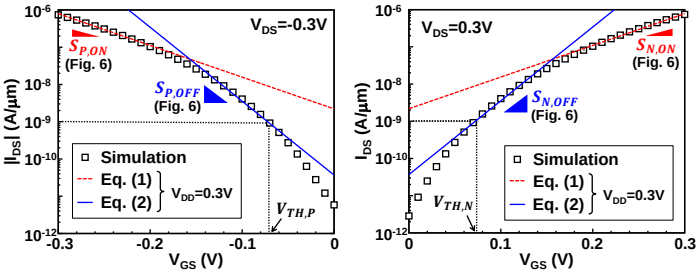
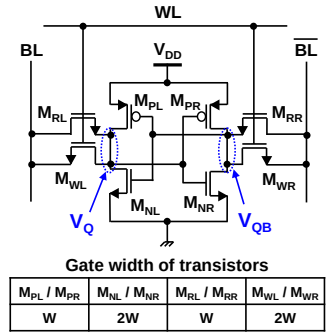


Fig. 2 (a) Cross-section of p-type TFET and (b) symbols of TFETs.



(a) characteristics of pTFET (b) characteristics of nTFET

Fig. 3. Simulated I_{DS}-V_{GS} characteristics of (a) pTFET and (b) nTFET. Two types of approximate characteristics (Eqs. (1) and (2) in Fig. 6) are also plotted. In this work, $V_{TH,N}$ and $V_{TH,P}$ are threshold voltages (V_{TH}) of nTFET and pTFET, respectively, and are defined as V_{GS} where $|I_{DS}|$ is 10^{-9} A/μm.



Gate width of transistors

M_{PL} / M_{PR}	M_{NL} / M_{NR}	M_{RL} / M_{RR}	M_{WL} / M_{WR}
W	2W	W	2W

Fig. 4 Schematic of an 8T TFET SRAM cell used in this work. W denotes a nominal gate width.

$$I_{DS} = I_{P(N)0,ON} e^{\frac{|V_{GS}|-|V_{TH,P(N)}|}{S_{P(N),ON}}} \left(1 - e^{-\frac{|V_{DS}|}{m_{P(N)}}}\right) \cdots (1) \quad I_{DS} = I_{P(N)0,OFF} e^{\frac{|V_{GS}|-|V_{TH,P(N)}|}{S_{P(N),OFF}}} \left(1 - e^{-\frac{|V_{DS}|}{m_{P(N)}}}\right) \cdots (2)$$

$$SNM_L = \frac{c}{c+1} S' \left(\frac{V_{TH,NR}}{S_{N,OFF}} - \frac{V_{TH,PR}}{S_{P,ON}} + \ln\left(\frac{S'c}{a}\right) - 1\right) - \frac{1}{c+1}\left(V_{TH,NL} - V_{TH,RL} + b\right) \cdots (3) \text{ (Proposed)}$$

$$\sigma(SNM_L) = \sqrt{\left(\frac{c}{c+1}S'\right)^2 \left(\frac{\sigma(V_{TH,NR})^2}{S_{N,OFF}^2} + \frac{\sigma(V_{TH,PR})^2}{S_{P,ON}^2}\right) + \left(\frac{1}{c+1}\right)^2 \left(\sigma(V_{TH,NL})^2 + \sigma(V_{TH,RL})^2\right)} \cdots (4)$$

$$P_{RF} = P\left(\min(SNM_L, SNM_R) < kT/q\right) \cdots (5) \quad (kT/q = 26\text{mV @ 300K}) \qquad \frac{1}{S'} = \frac{1}{S_{P,ON}} + \frac{1}{S_{N,OFF}}$$

Fig. 6. Equations used in this paper. **(1)** and **(2)** approximate I-V characteristics for TFETs (Fig. 3). $S_{P(N),0N}$ and $S_{P(N),OFF}$ represent the subthreshold swings at V_{DD} and $V_{DD}/2$ of pTFET(nTFET), respectively (Fig. 3). $m_{P(N)}$ is the saturation voltage constant of pTFET(nTFET) [5]. **(3)** Proposed analytical model of SNM_L. **(4)** Standard deviation of the SNM_L variation assuming that the V_{TH} variations are dominant. $V_{TH,NR}$, $V_{TH,PR}$, $V_{TH,NL}$, and $V_{TH,RL}$ are V_{TH}'s of M_{NR}, M_{PR}, M_{NL}, and M_{RL} in Fig. 4. a, b and c are parameters that depend on $I_{P(N),0N}$, $S_{P(N),0N}$, $S_{N,0FF}$ and $m_{P(N)}$. **(5)** Read failure probability (P_{RF}) defined in [2], where $P(X)$ is the probability that condition X is satisfied. Please note that SNM_R can be also derived in the same manner, but the detailed equations are omitted due to space constraints.

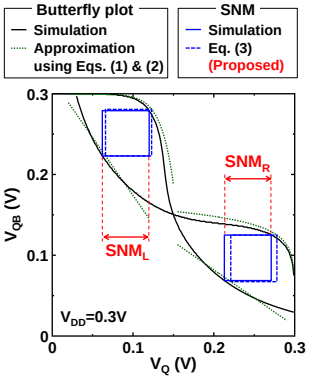


Fig. 5 Butterfly plot of the 8T TFET SRAM cell (Fig. 4) during read operation. SNM_L and SNM_R are defined as SNM in the upper-left and lower-right sides of the butterfly curves, respectively.

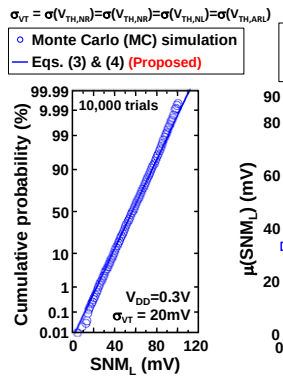


Fig. 7 Simulated and calculated cumulative probability of SNM_L.

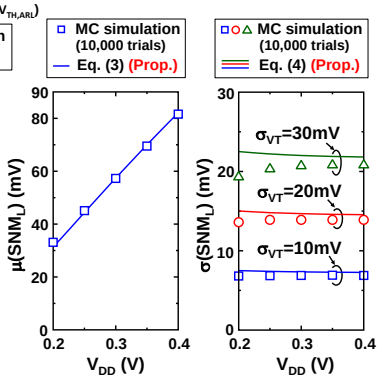


Fig. 8 Comparison of simulated and calculated SNM_L variations.

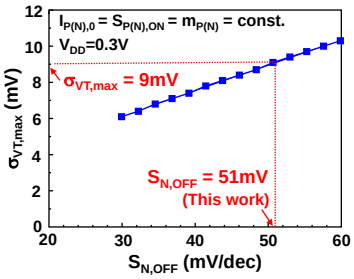


Fig. 9 $\sigma_{VT,max}$ (acceptable maximum σ_{VT} to satisfy $P_{RF}<10^{-6}$) as a function of the subthreshold swing $S_{N,OFF}$ (Figs. 3 and 6).

Table I Summary of device parameters.

	State-of-the-art process	Cost-effective process
Gate length L (nm)	20	65
Nominal gate width in SRAM (Fig. 4) W (nm)	60	300
EOT (nm)	1	1
Source doping N_S (cm^{-3})	2×10^{20}	2×10^{20}

Table II Sources of variation and σ's of them.

	State-of-the-art process	Cost-effective process
EOT [6] (nm)	0.013	0.013
N_S (*1) (cm^{-3})	1.05×10^{18}	3.16×10^{17}
Gate work function WF (*2) (meV)	30.6	9.30

(*1) $\sigma(N_S) = \sqrt{N_S/V}$, where V is the volume of the source region and is defined as $V = W^2 \times 50$nm (=depth of source region shown in Fig.2).

(*2) $\sigma(WF) = \frac{A_{VT(WF)}/\sqrt{2}}{\sqrt{LW}}$, and in this work $A_{VT(WF)}$ = 1.5 is used [7].

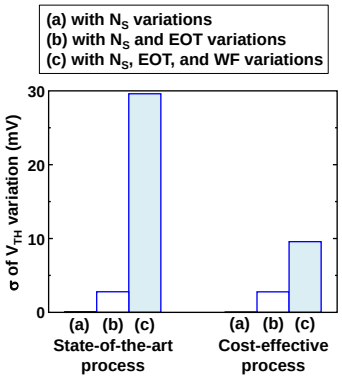


Fig. 10. Standard deviations (σ) of the V_{TH} variations caused by the sources listed in Table II.

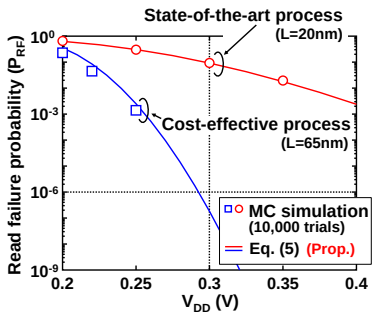


Fig. 11. Simulated and calculated read failure probability (P_{RF}) in two different processes. In the calculation by Eq. (5), it is assumed that the V_{TH} variation is dominant and is normally distributed.