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Performance Improvement in Lattice Matched SiGeSn/GeSn P-Channel TFET with Type-II Staggered Tunneling Junction

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Abstract

Lattice matched SiGeSn/GeSn hetero-PTFET with type-II staggered tunneling junction (TJ) is characterized by simulation. By tuning the material compositions, lattice matching and type-II band alignment at the Γ-point is obtained at SiGeSn/GeSn interface. Hetero-PTFETs demonstrate a steeper SS and an enhanced $|I_{ON}|$ compared to GeSn homo-PTFET, which is due to the modulating effect of staggered TJ on band-to-band tunneling.

1. Introduction

Recently, GeSn has attracted extensive research interests as a TFET material because of its direct band-to-band tunneling (BTBT) and easy integration on Si platform [1], [2]. Although, experimental and theoretical studies on GeSn TFETs have exploited great progress, there is still lack of the exploration of GeSn based TFETs with type-II staggered tunneling junction (TJ), which can improve the on-state current I_{ON} while maintain steep subthreshold swing (SS) and low off-state current I_{OFF} [3-9].

In this work, SiGeSn/GeSn hetero p-channel TFET (hetero-PTFET) with type-II staggered TJ is designed and characterized by simulation. The different compositions of GeSn and SiGeSn are chosen to provide type-II band alignment at the Γ-point as well as lattice matching. Significant performance enhancement is achieved in hetero-PTFETs over GeSn homo devices.

2. Band Structures of SiGeSn/GeSn and Device Simulation

The energy band structures of GeSn and SiGeSn were calculated utilizing the nonlocal empirical pseudopotential method (EPM) [Fig. 1 (a)]. SiGeSn and GeSn used in this work are direct bandgap materials. For GeSn, pseudopotential factors were taken from Ref. [10]. While for SiGeSn, the pseudopotential factors were adjusted to make the calculated bandgaps at Γ and L points consistent with the data obtained by formula (1) with bowing parameters listed in Table I,

$$E_{G,Si_{1-y-z}Ge_ySn_z} = E_{G,Si}(1-y-z) + E_{G,Ge}y + E_{G,Sn}z - b_{GeSi}(1-y-z)y - b_{GeSn}(1-y-z)z - b_{SiSn}yz \quad (1)$$

The band alignment at lattice matched SiGeSn/GeSn interface shown in Fig. 1(b) was calculated by Jaros' theory [11], which has been widely used to calculate the band offsets for many heterojunctions. Relative to the valence band of $Ge_{1-x}Sn_x$, the average valence band energies for $Si_{1-y-z}Ge_ySn_z$ are expressed as $0.69x-0.48y+0.69z$ eV [12].

Fig. 2(a) presents the schematic of SiGeSn/GeSn hetero-PTFET. Carrier effective masses used in simulation were extracted from full bands of materials calculated by EPM. Lattice matched SiGeSn/GeSn heterojunction with type-II staggered band lineup [Fig. 2(b)], is used as the source/channel TJ. 2D self-consistent device simulations were carried out utilizing TCAD simulator, which implements a dynamic nonlocal tunneling algorithm. Quantum confinement model provided by software was taken into account.

Table I Band parameters used in the calculation of band alignment at SiGeSn/GeSn interface [10], [12]-[14]

Valley	E_{Ge} (eV)	E_{Si} (eV)	E_{Sn} (eV)	b_{GeSi} (eV)	b_{GeSn} (eV)	b_{SiSn} (eV)
L	0.66	2.0	0.14	0.0	0.91	0.0
Γ	0.795	4.06	-0.413	0.21	2.1	13.2

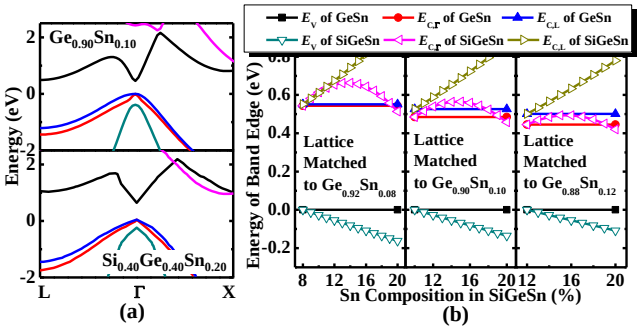

Fig. 1. (a) Energy band structures along L-Γ-X direction in the Brillouin zone of $Ge_{0.90}Sn_{0.10}$ (upper) and $Si_{0.40}Ge_{0.40}Sn_{0.20}$ (lower) calculated by the nonlocal EPM. (b) Band alignment for lattice matched $Si_{1-y-z}Ge_ySn_z/Ge_{0.92}Sn_{0.08}$, $Si_{1-y-z}Ge_ySn_z/Ge_{0.90}Sn_{0.10}$, and $Si_{1-y-z}Ge_ySn_z/Ge_{0.88}Sn_{0.12}$. Staggered heterojunction can be formed at SiGeSn/GeSn interface by increasing Sn composition in SiGeSn.

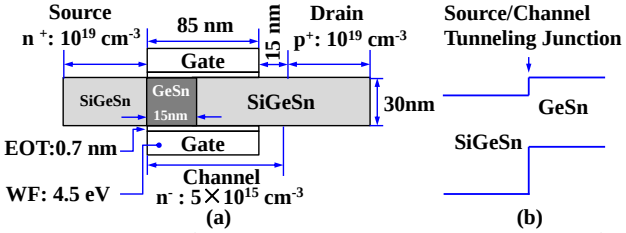

Fig. 2. (a) Schematic of SiGeSn/GeSn hetero-PTFET. (b) Schematic of the type-II staggered tunneling junction at source/channel interface.

3. Results and Discussion

Simulated $|I_{DS}|$-V_{GS} curves of lattice matched $Si_{1-y-z}Ge_ySn_z/Ge_{1-x}Sn_x$ hetero-PTFETs (x, y, z = 0.08, 0.33, 0.20, 0.10, 0.40, 0.20; and 0.12, 0.49, 0.20) and $Ge_{1-x}Sn_x$ homo devices (x = 0.08, 0.10, and 0.12) are shown in Fig. 3(a). Each hetero-PTFET demonstrates lower leakage floor current, sharper turn-on characteristic, and enhanced drive current over its corresponding homo control transistor. The improvement in point and average SS is achieved in hetero-PTFETs as compared to homo devices [Fig. 3(b) and 3(c)]. Point SS obtained at each V_{GS} is defined as $dV_{GS}/d(\lg|I_{DS}|)$. The higher maximum $|I_{DS}|$ with sub-60 mV/decade SS is achieved in hetero-PTFET over homo device [Fig. 3(b)]. Average SS is extracted from $|I_{DS}|$-V_{GS} curves, where V_{GS} various from V_{TH} to the value of V_{TH}-0.3 V. Here, the V_{TH} is defined as the V_{GS} at $|I_{DS}|$ of 10^{-10} A/μm. Fig. 3(d) compares the $|I_{ON}|$ of hetero-PTFETs and homo devices at $|V_{DD}|$=0.3V, showing that hetero-PTFETs achieve much higher $|I_{ON}|$ compared to the homo devices. An $|I_{ON}|$ of 22.87μA/μm is obtained in $Si_{0.31}Ge_{0.49}Sn_{0.20}/Ge_{0.88}Sn_{0.12}$ hetero-PTFET at $|V_{DD}|$ of 0.3 V, which is 2.3 times higher than that of $Ge_{0.88}Sn_{0.12}$ homo device, 9.94 μA/μm.

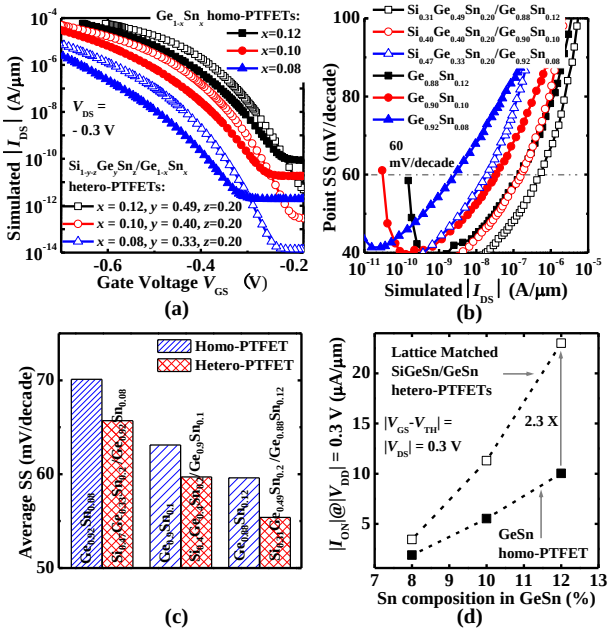

Fig. 3. (a) Simulated $|I_{DS}|$-V_{GS} curves for SiGeSn/GeSn hetero-PTFETs and GeSn homo devices. (b) and (c) indicating the superior SS in hetero-PTFETs over the GeSn homo devices. (d) Comparison of $|I_{ON}|$ for hetero and homo devices with different compositions at V_{DD} = - 0.3V. $Si_{0.31}Ge_{0.49}Sn_{0.20}/Ge_{0.88}Sn_{0.12}$ hetero-PTFET achieves 2.3 times higher $|I_{ON}|$ as compared to $Ge_{0.90}Sn_{0.10}$ homo-PTFET.

To illustrate the modulation effect of type-II staggered hetero-junction on the BTBT, energy band diagram and carrier density distributions are extracted. Fig. 4(a) compares the energy band diagrams along source to channel direction for the $Si_{0.40}Ge_{0.40}Sn_{0.20}/Ge_{0.90}Sn_{0.10}$ hetero- and $Ge_{0.90}Sn_{0.10}$ homo-PTFETs at $|V_{DD}|$=0.3 V. Both devices demonstrate a similar tunneling barrier, indicating the tunneling barrier is not much affected by the presence of hetero TJ at the fixed $|V_{GS}$-$V_{TH}|$. Fig. 4(b) depicts the carrier density profiles along source to channel direction at $|V_{DD}|$ of 0.3V. Hetero-PTFET achieves a more abrupt hole profile and a higher carrier density near TJ over the homo device. This also can be seen from the spatial distributions of carrier density [Fig. 5]. It has been reported that the more abrupt hole profile and higher hole concentration at TJ benefit the improvement of BTBT rate in TFETs. From Fig. 5, we can see that the central regions of hole density in hetero-PTFET are closer to TJ compared to homo device, which contributes to shorter tunneling path and higher tunneling probability.

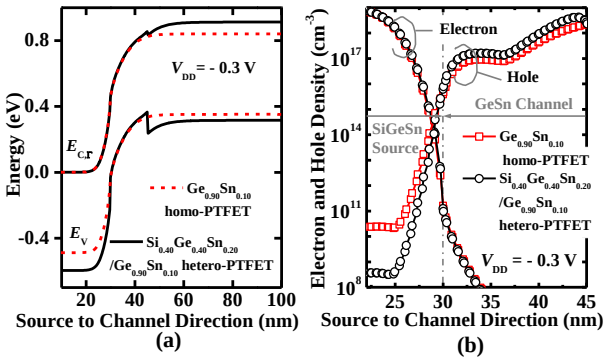

Fig. 4. (a) Energy band diagrams and (b) Carrier density profiles near surface along source to channel direction for $Si_{0.40}$ $Ge_{0.40}Sn_{0.20}/Ge_{0.90}Sn_{0.10}$ hetero-PTFET and $Ge_{0.90}Sn_{0.10}$ homo-PTFET at $|V_{DS}|$=$|V_{GS}$-$V_{TH}|$=0.3 V.

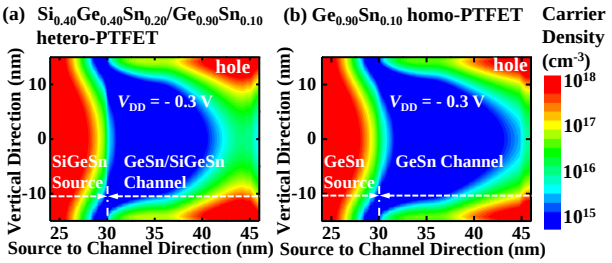

Fig. 5. Contour plots of carrier density for $Si_{0.40}Ge_{0.40}Sn_{0.20}/Ge_{0.90}Sn_{0.10}$ hetero-PTFET and $Ge_{0.90}Sn_{0.10}$ homo device at V_{DS}=V_{GS}-V_{TH}=-0.3V.

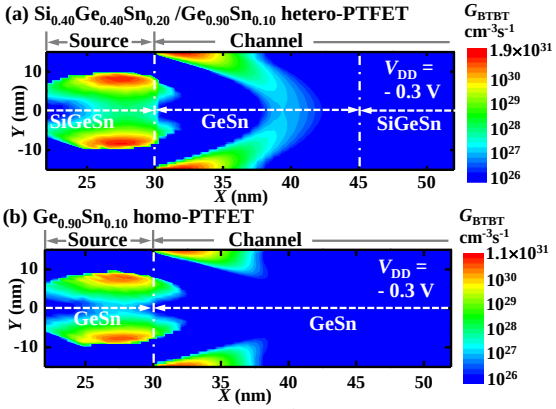

Fig. 6. Spatial distributions of G_{BTBT} for $Si_{0.40}Ge_{0.40}Sn_{0.20}/Ge_{0.90}Sn_{0.10}$ hetero-PTFET and $Ge_{0.90}Sn_{0.10}$ homo device at V_{DS}=V_{GS}-V_{TH}=-0.3V. The hetero transistor demonstrates a larger peak G_{BTBT} over homo device.

The impact of hetero-junction on BTBT of devices in on state is further analyzed by plotting the distribution of carrier generation rate G_{BTBT} (Fig. 6), which directly determines the magnitude of tunneling current. At $|V_{DD}|$=0.3V, $Si_{0.40}Ge_{0.40}Sn_{0.20}/Ge_{0.90}Sn_{0.10}$ hetero-PTFET demonstrates a higher peak value of G_{BTBT} compared to the $Ge_{0.90}Sn_{0.10}$ homo transistor. It is also noticed that the maximum G_{BTBT} centers in hetero-PTFET have a larger distribution area than that in homo device. We conclude that the aforementioned two points contribute to the enhancement of tunneling current in hetero device in comparison with the homo-PTFET.

4. Conclusions

SiGeSn/GeSn hetero-PTFET is designed and investigated. It is demonstrated that the modulation effect of type-II staggered hetero-junction on BTBT leads to a higher G_{BTBT} in hetero-PTFETs over the homo devices, which contributes to higher $|I_{ON}|$ and steeper SS in hetero-PTFETs.

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