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High performance low thermal budget Ge *n*- and *p*-MOSFETs by using ion implantation after germanidation technique

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Abstract

The device performance of Ge *n*- and *p*-MOSFETs by using ion implantation after germanidation (IAG) technique has been demonstrated. Dopant segregation at NiGe/Ge interface by low thermal budget drive-in annealing has an advantage in forming an abrupt metallic source/drain (S/D) junction. IAG technique is proved to be a low thermal budget process both for Ge *n*- and *p*-MOSFETs with high on I_{on}-I_{off} ratio and low parasitic resistance.

1. Introduction

Ge has been considered as a very promising channel material for replacing Si due to its higher carrier mobility than that of Si. Much improvement has been reported for Ge-based MOS devices over the past decade. However, it is still very challenging to achieve ultra-shallow junction as well as ultra-low parasitic resistance S/D on Ge due to the Fermi level pinning (FLP) between metal and Ge. With low thermal budget drive-in annealing, IAG technique has been thought an effective way to form ultra-shallow junction with reasonable I_{on}-I_{off} ratio on both *n*- and *p*-Ge.[1,2] To investigate the impact of IAG technique on total device performances, in this work, Ge *n*- and *p*-MOSFETs with self-aligned metallic NiGe S/D formed by IAG were fabricated. Both Ge *n*- and *p*-MOSFETs have shown excellent performance in terms of high I_{on}-I_{off} ratio, low parasitic resistance (R_{para}) and reasonable peak mobility.

2. Experimental

The schematic cross-section of Ge *n*- and *p*-MOSFETs is shown in Fig. 1. The detailed process flow is described as follows. After the native oxide was removed by a HCl solution, 4-in. *n*- and *p*-type Ge(100) wafers (n: 0.2-0.5 Ωcm, 5×10^{15} cm^{-3} p:0.5-1 Ωcm, 5×10^{16} cm^{-3}) were immediately loaded into a plasma-enhanced ALD chamber. Prior to a gate dielectric deposition, O_2 plasma treatment was conducted to form a GeO_x interfacial layer on Ge. Al_2O_3 gate insulator with the thickness of 5 nm was then deposited at 200 °C. Sputter-deposited TaN was patterned as gate electrodes by RIE. The oxide removal at S/D regions was carried out by BHF wet etching. Subsequently, IAG technique (Fig. 2) was performed as follows, a 10 nm Ni layer was deposited onto the S/D region followed by RTA at 350 °C to form self-aligned metallic NiGe S/D regions. Unreacted Ni was selectively etched in dilute HCl solution. An Al_2O_3 capping layer was deposited to protect the sample surface before the ion implantation. The condition of ion implantation set to confine the dopant in NiGe layer. After ion implantation, low thermal budget drive-in annealing at 350 °C is desirable for dopant segregation at the NiGe/Ge interface and contributes to the formation of an abrupt junction between the metallic S/D and Ge as shown in Fig. 3. Finally, a metallization was done as measurement pads.

3. Result and discussion

The drain current (I_D) – drain bias (V_D) characteristics of Ge *n*- and *p*-MOSFETs with 1 μm gate length (L_G) and 10 μm gate width (W) fabricated with IAG at 350 °C and 400 °C, respectively, are shown in Fig. 4. The maximum I_D of *n*- and *p*-MOSFETs are of ~170 and ~140 μA/μm at V_D of ±1.5 V and V_G of ±2 V, respectively. Fig. 5 shows the I_D-V_G and I_S-V_G transfer characteristics of Ge *n*- and *p*-MOSFET measured under V_D of ±50 mV and ±1 V. Both devices exhibited high on-off ratio of more than 10^4 and reasonable SS.

The relationship between measured resistivity (R_m) and effective channel length (L_{eff}) for varying gate overdrive values of Ge *n*- and *p*-MOSFETs fabricated with IAG is shown in Fig. 6 and Fig. 7. The lines that intersect at one point give the value of R_{para}. Considerably low R_{para} of 550 Ω-μm (Fig. 6) has been obtained on Ge *n*-MOSFETs even under the low thermal budget drive-in annealing at 350 °C. Owing to the effect of IAG, low R_{para} of 835 Ω-μm (Fig. 7) was also achieved on Ge *p*-MOSFETs after the optimization of drive-in annealing temperature at 450 °C. By using IAG technique, relatively low R_{para} have been achieved in both Ge *n*- and *p*-MOSFETs as compared with the state-of-the-art work (Fig. 8).

We also evaluate the impact of IAG technique on the carrier mobility in both Ge *n*- and *p*-MOSFETs. Fig. 9(a) and (b) show the effective electron and hole mobility of Ge *n*- and *p*-MOSFETs as compared with universal Si mobility. The peak electron mobility for Ge *n*-MOSFET has outperformed that of Si. However, the electron mobility at high Q_{inv} region degraded severely,[3] which may be improved by further enhancing the MOS interfacial quality. On the other hand, the hole mobility of Ge *p*-MOSFETs with 400 °C drive-in annealing is extremely higher than that of Si under the similar doping concentration. However, the effective hole mobility degraded after 450 °C annealing, which may be attributed to the low thermal stability of the GeO_x interfacial layer. IAG technique with low thermal budget annealing below 400 °C is suitable for fabricating high mobility Ge channel devices.

4. Conclusions

In conclusion, we demonstrate the effect of IAG in the device performance of Ge *n*- and *p*-MOSFETs. The results can be readily applied to scaled high mobility Ge CMOS with low thermal budget for achieving high I_{on}-I_{off} ratio and low R_{para}.

Acknowledgments

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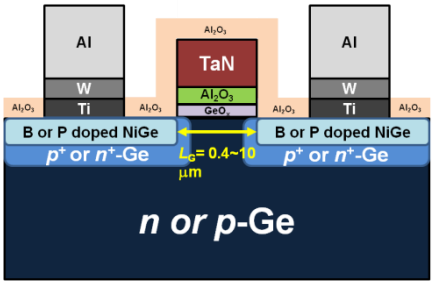

Fig. 1 Device schematic structure of Ge *n*- and *p*- MOSFETs by IAG.

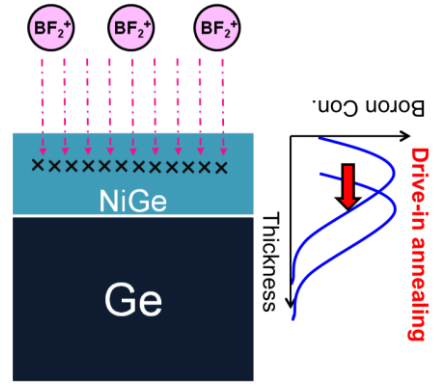

Fig. 2 The concept of ion implantation after germanidation (IAG) technique. Boron atoms will migrate and segregate at the NiGe/Ge interface after drive-in annealing.

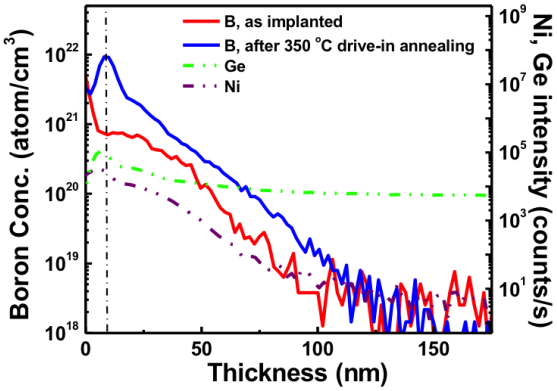

Fig. 3 Boron SIMS depth profiles before and after 350 °C drive-in annealing. The dashed line indicates the interface between NiGe and Ge.

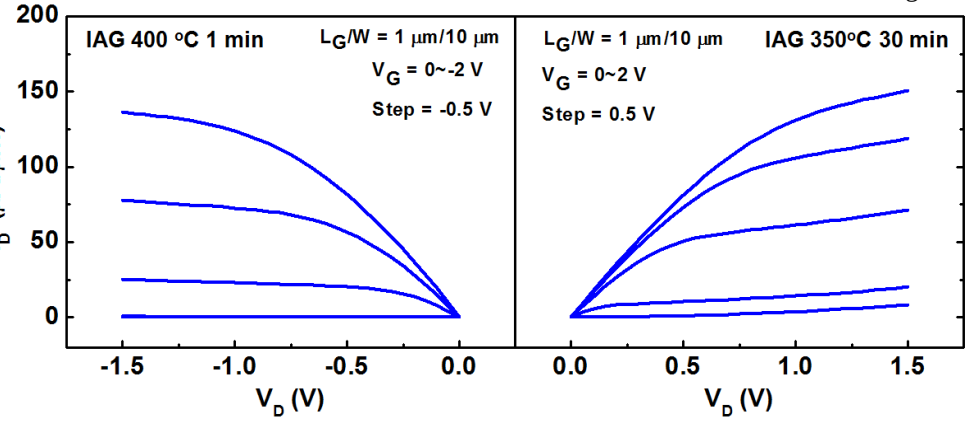

Fig. 4 I_D vs. V_D characteristics of Ge *n*- and *p*- MOSFETs fabricated by IAG with 1 μm L_G.

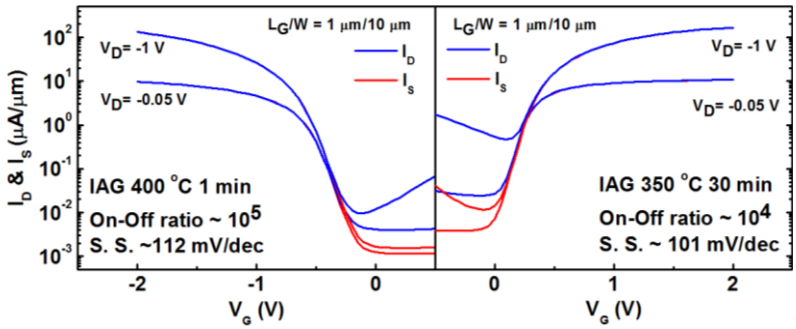

Fig. 5 I_D and I_S vs. V_G transfer characteristics of Ge *n*- and *p*-MOSFETs fabricated by IAG with 1 μm L_G.

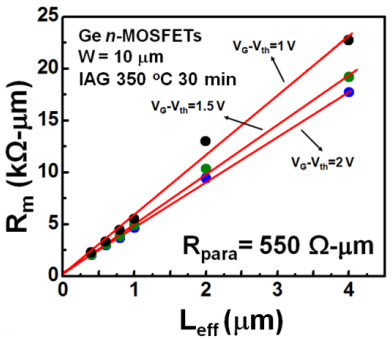

Fig. 6 Device measured resistance (R_m) vs. effective gate length (L_{eff}) at varying gate overdrives for Ge *n*-MOSFETs fabricated with IAG at 350 °C.

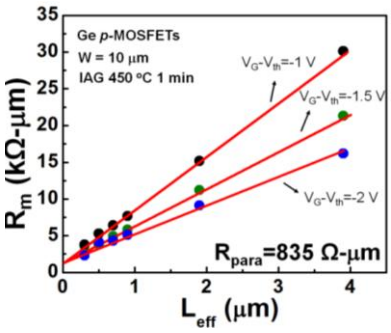

Fig. 7 R_m vs. L_{eff} at varying gate overdrives for Ge *p*-MOSFETs fabricated with IAG at 450 °C.

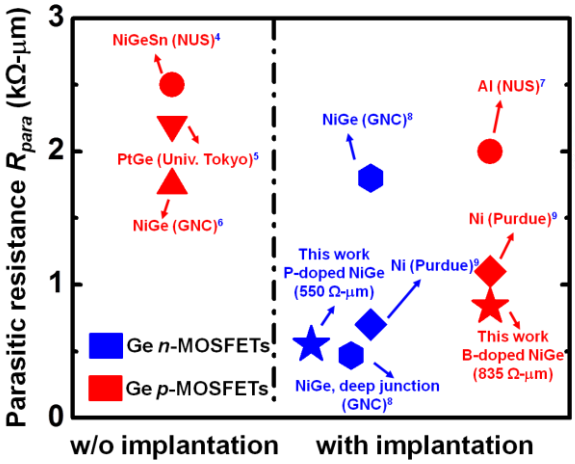

Fig. 8 Benchmark of R_{para} in the state-of-the-art planar Ge *n*- and *p*-MOSFETs. Material used for the S/D contact was pointed out.

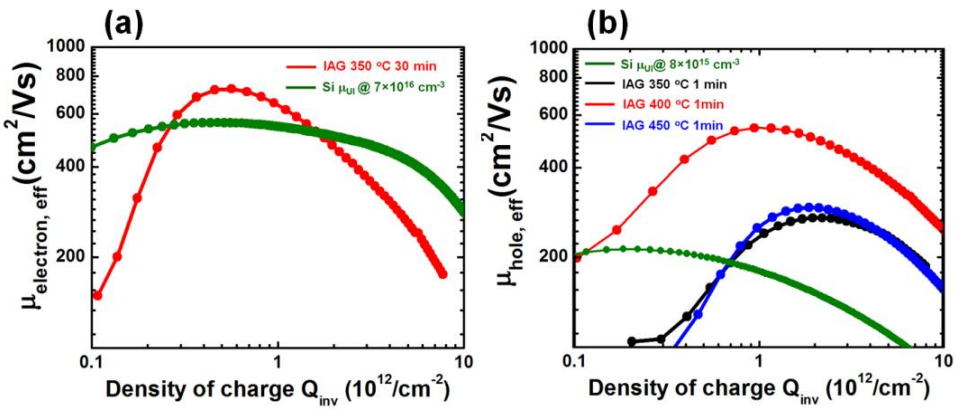

Fig. 9 Effective mobility of (a) hole and (b) electron for Ge *p*- and *n*-MOSFETs as compared with Si universal mobility.