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Steep-Slope Tunnel FET using InGaAs-InP Core-Shell Nanowire/Si Heterojunction

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Abstract

Tunnel FETs have attracted much attention as building-blocks for future low-power integrated circuits. Here we report on vertical tunnel FETs using InGaAs-InP core-shell nanowire/Si heterojunctions. The device demonstrates steep subthreshold-slope (SS ~ 42 mV/dec) turn-on behavior and very small DIBL at room temperature.

1. Introduction

Rapid increasing in power density of integrated circuits (ICs) with miniaturization of field-effect transistors (FETs) is serious problem. The main issue in future electronic circuits is lowering both off-state leakage current and subthreshold slope (SS) of FETs while enhancing the performance. The multi-gate structure such as fin-gate have been utilized to suppress the off-state leakage current. While, the reduction in the SS is difficult task since conventional FETs have a physical limit on SS due to carrier thermal diffusion mechanism (SS = 2.3 k_BT/q ~ 60 mV/dec). Further transistor' power scaling will be saturated by this limitation even if the GAA and surrounding-gate architecture are in practical use. Steep-slope transistors such as tunnel FETs (TFETs) and negative-capacitance FETs have, therefore, been emerged to beat the limitation.

The TFETs is most promising transistor for reducing SS under low bias [1]. The use of the TFET with SS below 60 mV/dec while keeping device performance as conventional FETs would reduce the required supply voltage < 0.5 V, compared with ~0.7 V needs by a conventional FETs. Although Si-based TFETs are attractive alternative structure for conventional FETs, precise control of doping and much strict gate-stack technology are required for reducing SS. Furthermore, the Si has low band-to-band tunneling efficiency resulting in low on-state current. In this regard, we have proposed the use of III-V/Si heterojunctions for TFET [2]. The benefit of the heterojunction is that staggered type-II band discontinuity is naturally formed across the III-V and Si junction regardless precise doping. And surrounding-gate architecture are available for the as-grown vertical III-V nanowires (NWs) on Si to obtain good gate-electrostatic control [3]. The heterojunction can also increase the tunnel current using strain effect.

Here we report on InGaAs NW/Si heterojunction TFET with surrounding-gate structure and characterize the effect of InP shell layer for the TFET property. The vertical TFET demonstrated steep SS (SS ~ 42 mV/dec) at room temperature and very small DIBL (~3 mV/V). And the current enhancement using the InGaAs-InP core-shell NWs was obtained.

2. Experimental details

2-1. Formation of InGaAs-InP core-shell NWs on Si by selective-area growth

The substrate was *p*-type Si(111) with carrier concentration of ~ 5 × 10^{-18} cm^{-3}. After 20 nm-thick SiO_2 was formed by thermal oxidation, openings were formed using electron beam (EB) lithography and wet etching. $In_{0.7}Ga_{0.3}As$ NWs were grown in low-pressure horizontal MOVPE system. We utilized specific growth sequence to align vertical InGaAs NWs on Si substrate [4]. Mono-silane (SiH_4) was used for n-type dopant, and Zn-pulse doping technique [5] was used to make pseudo intrinsic layer as channel region. The NWs were composed of Zn-pulse doped/Si-doped axial junction [Fig. 1(a)]. As for InP shell layer, we used lateral-over growth after the formation of the vertical InGaAs NWs. A typical growth result is shown in Fig. 1(b) and (c). Vertically aligned InGaAs NWs. The average diameter of the InGaAs NWs (d_c) was 100 nm. The diameter of the InGaAs-InP core-shell NW (d_{cs}) was 120 nm. Average NW length was 1.4 μm, and was same length after the InP shell growth. The typical lengths of Zn-pulse doped region and Si-doped region were 200 nm and 1200 nm, respectively.

2-2. Fabrication process for FET structure.

We fabricated a TFET with a single vertically aligned n^+-InGaAs/Zn-pulse doped InGaAs axial NW on a *p*-Si

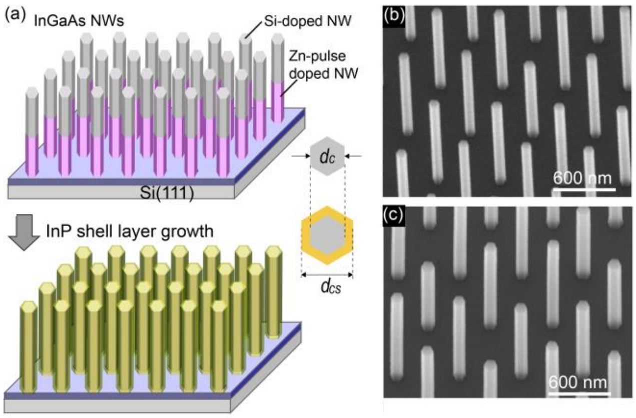

Fig. 1 (a) Illustration of InGaAs-InP core-shell NW growth. d_c and d_{cs} are diameter of InGaAs NW and InGaAs-InP core-shell NW, respectively. (b) 30º-tilted SEM showing growth result of vertical InGaAs NWs on Si. (c) 30º-tilted SEM showing growth result of vertical InGaAs-InP core-shell NWs on Si.

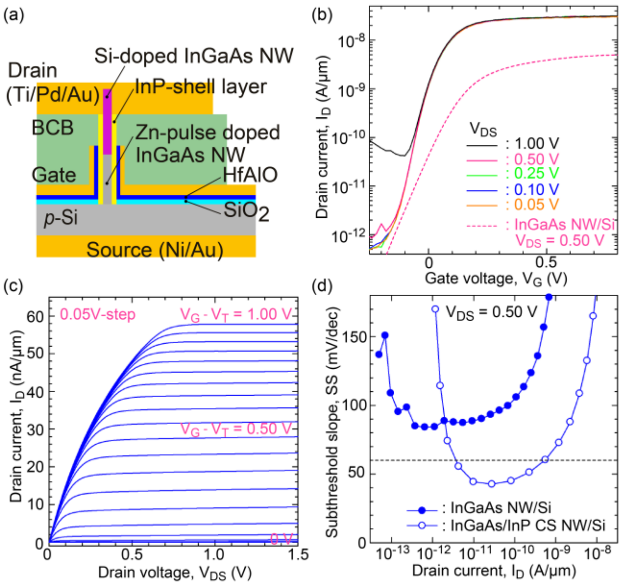

Fig. 2 (a) Illustration of vertical TFET structure. Gate length (L_G) was 200 nm. Thickness of HfAlO was 10 nm. The d_{cs} and d_c was 70 and 50 nm, respectively. The NW-length was 1.8 μm. The length of Zn-pulse doped segment was 200 nm. (b) Experimental transfer properties of the vertical TFET using InGaAs-InP core-shell NW/Si. The dashed curve represents that of TFET using InGaAs NW/Si heterojunction. (c) Experimental output characteristics of the TFET. (d) Subthreshold slope with a variation of I_D at V_{DS} = 0.50 V. The opened circle represents the TFET using InGaAs-InP core-shell (CS) NW and the closed circle is the TFET without InP shell layer. Dashed line is physical limitation of MOSFET (SS ~ 60 mV/dec).

substrate [Fig. 2(a)]. The carrier concentrations of the n^+-InGaAs and Zn-pulse doped InGaAs were 1.0×10^{19} and 3.5×10^{15} cm^{-3}, respectively. The d_{cs} and d_c was 70 and 50 nm, respectively. The thickness of the InP was 10 nm. The device processes for the TFET were the same as previously reported [5]. First, the NW was covered with 10-nm-thick $Hf_{0.8}Al_{0.2}O_x$ by using atomic-layer deposition. Next, tungsten (W) gate-metal was deposited by RF sputtering and patterned the gate region by wet process. BCB was then spin-coated on the NW. Subsequently, the BCB and the W were etched by RIE at the same time. Next, the top part of the 500 nm-long NW was revealed. Then, the device was spin-coated again with BCB for electrical isolation between the gate-metal and drain-metal. The L_G was 200 nm, which approximately corresponds to the length of the Zn-pulse doped NW segment (channel length). After the RIE, Ti/Pd/Au multilayer were evaporated as drain and Ni/Au was deposited on backside of *p*-Si to serve as source electrodes. Finally, the device was annealed at 420°C for 2 min in N_2.

3. Results and discussion

Figure 2(b) shows representative transfer properties of the InGaAs-InP core-shell NW/Si TFET at drain-source voltage (V_{DS}) of 0.05 – 1.00 V. The curve was measured using parameter analyzer (Agilent 4156C) at room temperature in the dark. The measured current was normalized using gate-perimeter. Switching behavior with a SS of 42 mV/dec was obtained under reverse bias direction (V_{DS} is positive against *n-i-p* junction). This switching characterization appeared at as low as V_{DS} of 10 mV. The SS of the TFET exhibits steeper SS behavior under various V_{DS}. The ratio of the I_{ON}/I_{OFF} current was approximately 2.5×10^4 at V_{DS} of 0.50 V. The on- and off-state currents were about 2.5×10^{-8} and 1.0×10^{-12} A/μm, respectively. The threshold voltage, V_T, of the I_{DS} was -0.10 V. Fig. 2(c) show output characteristic of the device indicating the dark Zener current of the diode structure was modulated by the V_G. The saturation region appeared with a function of $(V_G)^{-1}$ in Fig. 2(c). The I_{ON} was ~ 27 nA/μm at V_{DS} = V_G-V_T = 0.50 V. The DIBL was 3 mV/V, which is much smaller than the conventional MOSFETs. This indicates the internal electrical field is applied at tunneling junction regardless of surface potential lowering due to V_{DS}. Instead, I_{OFF} due to tunneling leakage was increased at V_{DS} = 1.00 V.

The pink dashed curve in Fig. 2(b) was transfer property of bare InGaAs NW/Si TFET at V_{DS} = 0.50 V. The TFET using the bare InGaAs NW showed SS of 80 – 90 mV/dec [closed circles in Fig. 2(d)] and the I_{ON} was 2.7 nA/μm. The I_{ON} for InGaAs-InP core-shell NW/Si TFET was 10 times higher than that of the bare InGaAs NW/Si TFET. The benefit of using InP shell layer is improvement of SS and enhancement of I_{ON}. The InP shell layer act as passivation effect on the semiconductor/oxide interface [7], which decreases interface-state density, and thus resulted in electrostatic improvement of the SS below 60 mV/dec. Strain effect of the InP shell layer also contributes to the improvement of SS and I_{ON} as well as the passivation effect. The outer InP shell induces biaxial compressive strain against the whole core-InGaAs NW due to the lattice mismatch (-1.16%), and this ascribes that the uniaxial tensile strain localized at the near tunneling junction (InGaAs/Si junction). The tensile strain lowers conduction band minimum of the core InGaAs NW [7] and then decreases effective energy-gap across Si and InGaAs junction. The lowered energy-gap increases tunneling probability and I_{ON}.

4. Conclusions

We have demonstrated vertical TFET using InGaAs-InP core-shell NW/Si heterojunction. The InP layer had both passivation and strain effect on the TFET properties. The device showed steep SS (~ 42 mV/dec) turn-on behavior and current enhancement which was 10 times higher than that of the TFETs without InP shell layer. The TFET with steep SS exhibits very small DIBL (~3 mV/V). Next issue is to realize very high I_{ON} with smaller SS by using scaling of channel length and realization of coherent growth.

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