Effect of 3D Current Distribution in the Characterizing Parasitic Resistance of FinFETs
Po-Yen Lin1, Yu-Lun Chiu1, Fan-Hsuan Meng 1,Kuang-Hsin Chen2, Serena Hao2, Bor-Zen Tien2, Tzon-Sheng Chang3, Chron Jung Lin1 and Ya-Chin King1
1Microelectronics Laboratory, Institute of Electronics Engineering, National Tsing Hua University, Hsinchu300,Taiwan
2Process Integration Division, Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan
Phone/Fax:+886-3-5162219, E-mail: ycking@ee.nthu.edu.tw

Abstract
A novel technique for the analysis of 3D current distribution and crowding effects in FinFETs is presented. Through combining data from multiple characterizing techniques on new test pattern designs, the key components which contribute to FinFETs’ parasitic resistance can be quantified. Through a 3D resistive network model, further understanding of current distribution/flowing vectors in this vertical and lateral direction in the source/drain epitaxial region are thoroughly analyzed. This technique identifies key components which contribute to the parasitic resistance, limiting the overall driving capability in non-planar transistors.

Keywords: FinFET, Parasitic Resistance, 3D resistive model

1. Introduction
To scale CMOS field-effect transistors (FETs) well into the sub-20nm regime, multi-gate structures, such as FinFET, double gate and surround gate structures, becomes the mainstream technology. However, epitaxial S/D regions and aggressively scaled channel length lead to enhanced parasitic effects. The serious parasitic resistance and capacitance degrades the overall device performance and limits the circuit speed in scaled of CMOS ICs [1]. In the past decades, several extraction methodologies for characterizing the parasitic resistance from the total device resistance has been developed [2]. These conventional methods generally assume constant channel mobility and constant effective channel length under various bias conditions and in all conduction regimes. When one applied these methods to FinFET devices, inaccurate results owning to short-channel effects [3] and apparent current-crowding effects become problematic to device engineers. In this work, multiple characterization methods on a series of test patterns including traditional Kelvin Structures and Cross Bridge Kelvin Structures [4, 5] are discussed and verified experimentally by a FinFET technology. The new extraction methods become insensitive to constant mobility and Leff assumptions, hence accurate and consistent results are obtained, giving a practical overview of parasitic resistance in non-planar CMOS transistors.

2. Device Structure and Resistance Component
In Fig. 1, TEM picture shows cross-sectional view of a FinFET device consist with epitaxial source/drain and serial parasitic resistances are also outlined. In fact, epitaxial source/drain region is designed with expanded volume in order to reduce series resistance. This unique structure leads to non-uniform current distribution in the epitaxial region, when current flows through expanded source/drain to a narrow channel. The parasitic resistance (R_p) is conventionally extracted through channel modulation method (CMM) under low drain condition of 50mV. By assuming the R_p is independent of overdrive voltage (ΔV), its value can be extracted by extrapolation at 1/ΔV=0. Data shows that device with multiple fins exhibits proportionally smaller series resistance, as summarized in Fig. 2. Extracted R_p vs. number of fins shows good linear dependency, as expected by first order model. As outline in the inset of Fig. 3, key components for series resistance in a FinFET includes, LDD resistance (R_{LDD}), contact resistance (R_c) and source drain resistance (R_{SD}).

3. Series Resistance Extraction and Characterization
To further understand and quantify each component which contributes to R_p, a series of test patterns are designed and measured. By obtaining the R_p of FinFETs with different contact-to-gate spacing, one can easily extract the R_{LDD} component which is proportion to the spacing. The rest can then be estimated by extrapolation at spacing equals to zero. In Fig. 4, the slopes of resistance vs. spacing is found to be identical under different ΔV, which proves that R_{LDD} is linearly proportion to contact-to-gate spacing, as expected. Specific contact resistance, R_c, is independently characterized through both lateral and vertical Kelvin structures. Measurement data in Fig. 5 reveal that the laterally flowing current can lead to significantly large R_c. We believe that this is caused by worse crowding effect in lateral contact structure.

To investigate the difference in R_p between lateral and vertical current flowing conditions, a diode extraction method (DM) is proposed. Fig. 6 shows the measured diode forward biased IV characteristics. The parasitic resistance consists of R_p+R_{pp} (R_{pp} lumps up all serial pick-up resistance) dominate IV curve in the high current level regimes, as indicated in Fig. 6. The test pattern consists of two closely placed pn junction as illustrated in Fig. 7 (a). By applying a fixed current through one and two forward junctions, respectively, and monitoring the terminal voltage on one junction. R_{pp} can be extracted by (V_i+V_j)/(I) (see Fig. 7(b)) and hence the remaining R_p= R_{pp} is obtained .

Fig. 8 (a) compares R_p and R_{pp} obtained by CMM and DM, R_p in DM is larger than CMM when they both normalize to the same distance 17nm. This might be caused by the non-uniform SiP concentration along the epitaxial region. Fig. 8 (b) summarizes source contribution to the total resistance to FinFET, which are broken down into four main component, where R_c is the dominant component the overall R_p.

4. Analysis of Current-Crowding Effect and Temperature Effect
To further understand the impact of non-uniform current flow on R_p, a 3D FinFET resistance model describing the channel/3D extension and epitaxial region is built, as demonstrated in Fig. 9. The current is found to spread out in the large epi-region when enter from the contact. Then, it is confine to the thin extension region and finally flow to the other side through H-like surface channel. Based on this 3D model, the current distribution along the z-direction of different depth level is obtained, see Fig. 10. Non-uniform current distributioncan lead to serious crowding effect as the surface layers. To analyze the complete current distribution along z and y direction, respectively. Figure 11 summarize the percentage of layer current at different depths and width. Results indicate that with a contact at the epi surface, current flow through the bottom channel region can be 30% lower that at the top. Data in the y-direction suggest that the extended epi region wider than fin has very limited effect on increasing current handling capability, epi growth in the y-direction are very effective in reducing the overall R_{ds}.

To improve the non-uniform current distribution problem, epi regions with a retrograde doping profile is designed, see Fig. 12(a). Simulation data in Fig. 12(b) reveal that uniform current distribution in z-direction can be achieved. In addition, a recess contact, as illustrated in the inset of Fig. 13, is found to alleviate current-crowding effect and effectively reduce R_p. Simulation results in Fig. 13 show up to 20% reduction in R_p can be achieved with a recess depth of 10nm.

Self-heating in FinFET devices is known to be a critical problem [6]. Hence, temperature dependency of parasitic resistance can lead to additional performance shifts in ICs may occurs in high-driving condition. In Fig. 14, both lateral and vertical-current-crowding resistance show minimal change with temperature. As revealed by data in Fig. 15, since channel resistance shown a strong positive temperature dependence, the overall drive current change can be compensated by the negative temperature dependency in R_p.

5. Conclusions
By combining conventional and novel characterization techniques for parasitic resistance extraction, key components which contribute to its parasitic resistance are independently quantified. A 3D resistive network provides further insights into the non-uniform current distribution in the epitaxial region during channel conduction. The temperature effect on parasitic resistance is also addressed. These detail analysis enable new device structure optimization and/or process modifications to further enhance overall device performance.

References
Fig. 1 The cross-sectional view of a FinFET device with its resistance model.

Fig. 2 Parasitic resistance ($R_p$) extraction through channel modulaiton method at low drain of 50mV.

Fig. 3 Extracted $R_p$ vs. number of fins (NF) shows good linear dependency.

Fig. 4 Total resistance of FinFETs vs. contact-to-gate spacing reveals good linear dependency.

Fig. 5 Specific contact resistance can be measured by both lateral and vertical Kevin Structure.

Fig. 6 At high current regime, diode current can be used for $R_p$ extraction.

Fig. 7 (a) Extraction of $R_c+R_{sd}$ by applying one or two diode current. (b) The voltage difference, $\Delta V=V_2-V_1$, where $R_{pp}$ can be extracted by $\Delta V/I$.

Fig. 8 (a) Comparison of $R_c$ and $R_{sd}$ under vertical and lateral current flow. (b) Analysis reveals that $R_c$ accounts for more than 20% of the total resistance.

Fig. 9 3D resistance model for FinFET analyzing current distribution in the epitaxial to channel region.

Fig. 10 Current distribution at different depth into the z-direction. Non-uniform current distribution can lead to serious crowding effect.

Fig. 11 Current flow through the bottom channel region is lower that at the top. While extended epi region carrier only small portion of current flow.

Fig. 12 (a) Retrograde doping profile in epi region. (b) Uniform current distribution can be obtained to avoid crowding effect.

Fig. 13 Recess contact can effectively reduced $R_p$.

Fig. 14 Temperature dependency of contact resistance. Both lateral and vertical $R_c$ show minimal temperature dependence.

Fig. 15 $R_a$ depends strongly with temperature change. Overall transistor current compensated by $R_p$ exhibits less temperature dependency.