High Performance 14nm SOI FinFET Technology

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Abstract
We present a fully integrated 14nm CMOS technology featuring FinFET architecture on an SOI substrate for a diverse set of SoC applications including HP server microprocessors and LP ASICs. This SOI FinFET architecture is integrated with a 4th generation deep trench embedded DRAM to provide an ultra-dense (0.0174μm²) memory solution for industry leading ‘scale-out’ processor design. A broad range of Vt's is enabled on chip through a unique dual workfunction process applied to both NFETs and PFETs. This enables simultaneous optimization of both lowVt (HP) and HiVt (LP) devices without reliance on problematic approaches like heavy doping or Lgate modulation to create Vt differentiation. The SOI FinFET’s excellent subthreshold behavior allows gate length scaling to the sub 20nm regime and superior low Vdd operation. This leads to a substantial (>35%) performance gain for Vdd ~0.8V compared to the HP 22nm planar technology. At the same time, the exceptional FE/BE reliability enables high Vdd (>1.1V) operation essential to the high single thread performance for processors intended for ‘scale-up’ enterprise systems. A hierarchical BEOL with 15 levels of copper interconnect delivers both high performance wire-ability as well as effective power supply and clock distribution for very large >600mm² SoCs [1].

1. Technology Description and eDRAM

The critical dimensions for this 14nm technology are shown in Table 1. The process flow, along with key device cross sections, is shown in Fig 1. The 42nm fin pitch is achieved using sidewall image transfer. The SOI substrate provides multiple advantages for overall FinFET integration. Use of an SOI substrate 1) minimizes the process complexity associated with both fin isolation and eDRAM integration, 2) minimizes the parasitic capacitance at the base of the fin, 3) simplifies patterning of the active fins, and 4) minimizes each component of fin structural variability (i.e. height, thickness, and profile).

Table 1 Key technology scaling rules and attributes.

<table>
<thead>
<tr>
<th>Level</th>
<th>Pitch</th>
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<tbody>
<tr>
<td>Fin</td>
<td>42nm</td>
</tr>
<tr>
<td>Gate (single pattern w/ cut)</td>
<td>80nm</td>
</tr>
<tr>
<td>Contact</td>
<td>80nm</td>
</tr>
<tr>
<td>M1 (Bi-directional)</td>
<td>64nm</td>
</tr>
<tr>
<td>Mx</td>
<td>64nm</td>
</tr>
<tr>
<td>BE Hierarchy: 1X,1.25X,2X,4X,8X,40X</td>
<td></td>
</tr>
<tr>
<td>eDRAM cell area</td>
<td>0.0174 μm²</td>
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</table>

Fig. 1 Process flow and cross sections for 14nm SOI FinFET technology.

One of the key advantages of the SOI substrate is the ability to co-integrate deep trench eDRAM with logic. The unit cell has been scaled down to 0.0174μm², which provides a unique memory solution for cache starved processors (Fig. 2). This cell scaling and performance have been enabled by the FinFET. The SCE improvement achieved in the pass gate has allowed for significant reduction of both Lgate and Vt, without compromising retention specifications.

Fig. 2 eDRAM area scaling over the last four generations culminating in the 0.0174μm² cell in 14nm SOI FinFET technology.

2. Transistor Performance and Scaling

The SOI FinFET architecture enables a SCE that is well controlled down to the sub-20nm Lgate (Fig. 3). This device behavior, coupled to the optimized fin height selection and parasitic capacitance optimization, has resulted in a performance improvement of >35% over the predecessor 22nm technology node at lower operation voltage at 0.8V [2].

Fig. 3 DIBL response of 14nm SOI FinFETs compared to 22nm SOI planar devices. SCE control is demonstrated down to the sub-20nm Lg.
3. Multiple Vts and Dual-WF

The simplest way to achieve wide range of Vt in the FinFET technology is through channel doping. However, high doping concentrations in FinFETs reduces carrier mobility and increase random dopant fluctuations, thereby degrading the performance of lower leakage transistor. This limit the use of channel doping up to a few $10^{18}$ cm$^{-3}$ (Fig. 4) [3].

In this work, we apply an innovative dual WF process to generate widely spaced Vts (for both N/P) without reliance on doping to create the Vt separation. The dopant removal enables 1) significant performance enhancement for HiVt (LP) devices due to the mobility gain (thus device DC performance gain, Fig. 5-6) and 2) significant Vt mismatch (Vmin) reduction for low leakage SRAM cells due to the RDF reduction (Fig. 7).

4. Reliability for High Performance Server Application

The TDDB result for this technology are shown in Fig 8. Both TDDB and BTI pass the specifications required to support 10 year lifetime at $V_{max} > 1.1$V. This technology provides up to 15 levels of Cu metallization. The hierarchical BEOL architecture begins with 64nm pitch at M1/Mx and expands up to ultra thick levels required for efficient clock and power distribution across a >600mm$^2$ chip. Throughout the BE, metallization processes have been developed so that wire resistance and EM lifetime can be optimized simultaneously.

5. Conclusions

A HP 14nm SOI FinFET technology has been developed featuring >35% performance improvement, an ultra-dense 0.0174um$^2$ embedded DRAM memory cell, and dual WF gatestack enablement that achieves optimized HP and LP devices simultaneously on chip.

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References