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Transistor-level Characterization of SRAM Bit Failures Induced by Random Telegraph Noise

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Abstract

Bit failure events induced by random telegraph noise (RTN) for silicon-on-thin-BOX (SOTB) SRAM cells was characterized by directly monitoring the storage node voltage of individual cells, using a device-matrix-array (DMA) TEG. Correlating the cell level RTN/failure waveforms with that of individual transistors that constitute the same cell, RTN of a specific transistor that causes the cell failure was identified.

1. Introduction

RTN [1] is a serious reliability concern for scaled MOS transistors. RTN is caused by a small number of traps, which are inherent in gate dielectric materials, and cannot be easily removed. This is in contrast to random-dopant-fluctuation (RDF), which can be effectively reduced by using non-doped SOI or FinFETs. Impact of RTN increases as transistors are scaled, and V_{TH} shift as large as 100mV is reported [2]. The reliability of SRAMs using small transistors is easily affected by RTN [3-7], in particular, for low voltage operations.

Usually, SRAM failure due to RTN is evaluated using memory testers and functional memory macros with normal cells. In this case, it is not possible to correlate bit failures and RTN of individual transistors. To overcome this limitation, in this work, an addressable device-matrix-array (DMA) TEG is used. By directly measuring the node voltage of SRAM cells and the characteristics of individual transistors that constitute the same cells, specific device level RTN that causes cell failure events can be identified.

2. Measurement Results

In this work, a 6T-SRAM DMA-TEG [8] fabricated by a 65nm fully depleted SOTB technology [9,10] is used. The TEG is designed such that the storage nodes (VL and VR of Fig.1) of each cell are directly accessible, allowing the measurements of the node voltage under cell operation, as well as individual transistor I-V characteristics. Thanks to the low V_{TH} variability of the non-doped channel architecture, SOTB SRAMs can achieve very low minimum operation voltage (V_{MIN}) of 0.37V [10], which is much lower than bulk SRAMs [11]. Fig.2 shows the distributions of measured noise amplitude ΔV_{TH} of 1k cell transistors. pFETs show about twice as large ΔV_{TH} as nFETs.

Fig.3 shows the SRAM cell measurement sequence. After writing VL=High or VL=Low with sufficiently high voltage, V_{DD} was lowered to 0.2V and the node voltage VL and VR were monitored with $V_{DD}=V_{BLL}=V_{BLR}=V_{WL}=0.2V$ (read disturb condition). As a result, sudden jumps of VL and VR (i.e. bit failure) were found in 5 out of 1k cells. Then, one of the failed cells was selected for further detailed analyses.

Fig.4a shows measured node voltage waveforms of the selected cell. The data (VL=high) initially retained suddenly flipped after 53s (i.e. time to flip τ_F is 53s). Fig.5 shows the statistical distribution of τ_F obtained by repeating the measurement as in Fig.4. Note that, before the flip, small noise is observed for both VL and VR (Fig.4b).

Fig.6 shows the measured butterfly curves of the cell, which confirms that the VL=high state is only marginally stable. In addition, by repeating the measurement, it was found that the curve for the left inverter is split into multiple lines, indicating the existence of RTN in either TpL, TaL, or TnL in Fig.1. In an extreme case, VL=high stable point appears to be lost, as shown in Fig.6b.

To determine the transistor responsible for the noise, individual transistor characteristics were measured. It was found that the drain current vs time of TpL, biased near the stable point of interest, exhibit clear multiple-trap RTN (Fig.7). The similarity of the waveforms and the consistency of the amplitudes in Fig.4b and Fig.7 indicate that the noise in Fig.4 is caused by the RTN in TpL. These results clearly show that the RTN in TpL diminish the cell stability to a critical level as in Fig.6.

Finally, it can be shown that the TpL RTN is indeed triggering the data flip, or bit failure. TpL current occasionally drops below 0.26μA, as shown by the arrow in Fig.7. Fig.8 compares statistical distributions of τ_F (Fig.5) and the time to the current drop below 0.26μA. The good agreement strongly suggests that the low-side spike of the TpL RTN triggers the SRAM cell failure.

3. Conclusions

Using a specially designed DMA-TEG, SRAM cell failure events can be directly measured and correlated with the individual cell transistors. The noise signal of a transistor responsible for the data flip was clearly identified.

Acknowledgements

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References

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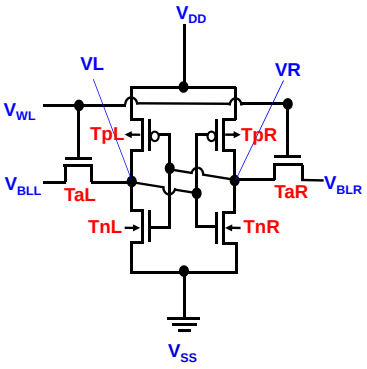

Fig.1. Definition of node and transistor names of an SRAM cell.

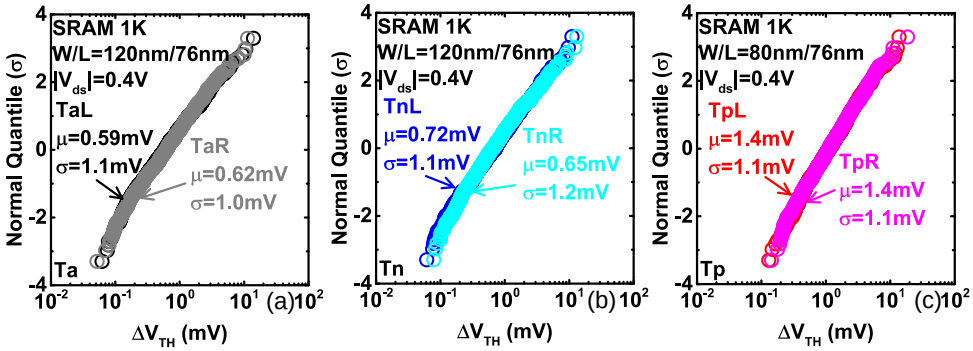

Fig.2. Measured ΔV_{TH} distributions of (a) access nMOS (TaL, TaR), (c) driver nMOS (TnL and TnR), and (d) pMOS (TpL, TpR) of 1K FD SOTB SRAM cells.

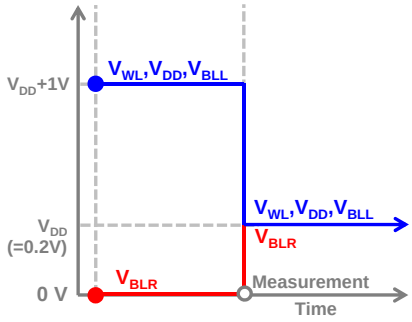

Fig.3. Voltage sequence of the measurements in VL=High case.

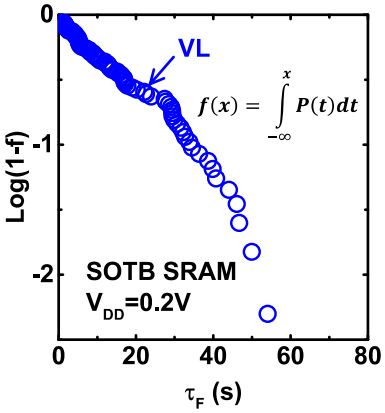

Fig.5. Distribution of measured τ_F where τ_F is time-to-failure.

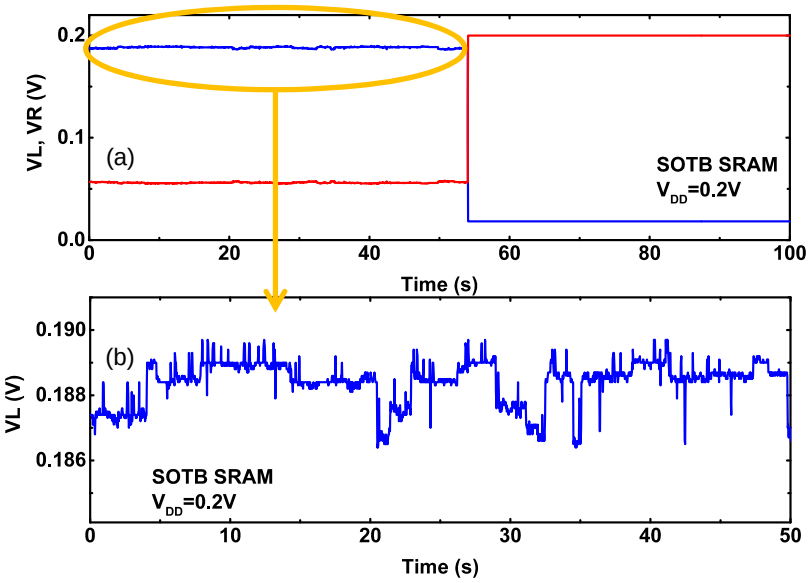

Fig.4. Example of measured VL and VR waveforms exhibiting bit failure at t=53s. (a) full view and (b) magnified view of small noise signal before failure.

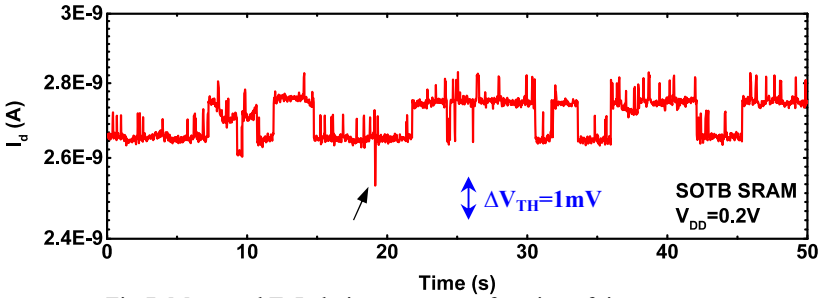

Fig.7. Measured TpL drain current as a function of time.

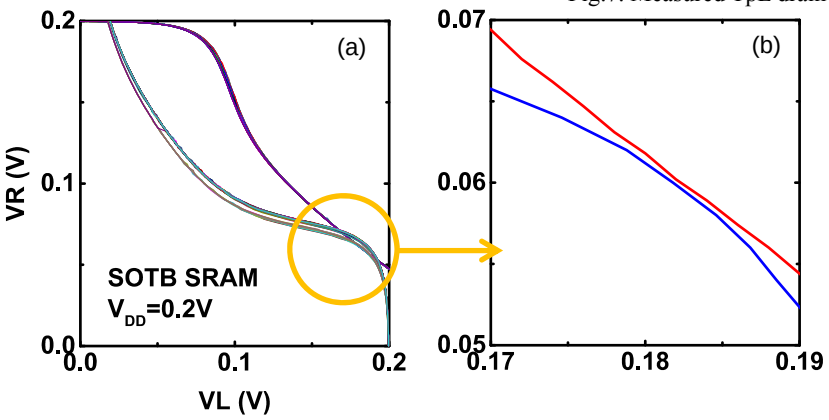

Fig.6. (a) Repeatedly measured butterfly curves of the cell shown in Fig.4. (b) Magnified view of the curves that happen to lose intersection.

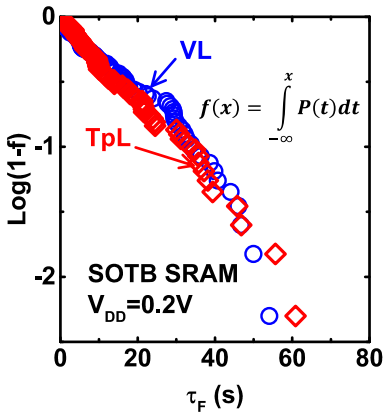

Fig.8. Distributions of measured τ_F and time to negative Id spike in Fig.7.