1/f Noise in Submicron Top-Gate Crystalline Oxide Semiconductor FET

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Abstract

The 1/f noise in a submicron top-gate crystalline oxide semiconductor FET typically, a c-axis aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO) FET (CAAC-IGZO FET) is analyzed. It is found that the 1/f noise with channel lengths of 0.35 to 0.8 µm is described by a mobility fluctuation model. The 1/f noise in CAAC-IGZO FET has trends of a lower noise level, lower probability of causing fluctuations in carrier number, and weaker temperature dependence than NMOS (Si) FET; thus, the CAAC-IGZO FET is effectively applied to analog LSIs.

1. Introduction

A crystalline oxide semiconductor FET, typically, a c-axis aligned crystalline Indium-gallium-zinc oxide (IGZO) FET (CAAC-IGZO FET) has extremely low off-state current [1]. This motivated the development of a CAAC-IGZO FET for high-resolution low-power displays [1] and LSI such as the field programmable gate array [2].

In a recent study, we have focused on analog LSI applications that can benefit from the extremely low off-state current of CAAC-IGZO FETs, e.g., global shutter image sensors [3, 4] and a VCO that uses analog memory [5]. Analog LSIs, especially, image sensors require scaling FETs down to the submicron scale, which makes a proper understanding of noise important. Some studies reported on the 1/f noise (flicker noise or low-frequency noise), a basic device parameter, in the IGZO FET; however, these were interested in devices on the order of a micron [6-8].

In this study, the 1/f noise in submicron top-gate CAAC-IGZO FET is analyzed. It is shown that the 1/f noise characteristics of the CAAC-IGZO FET seem superior to those of the NMOS (Si) FET; the 1/f noise level is lower, it does not result in fluctuations in carrier number, and has weaker temperature dependence. These characteristics make it effective to use CAAC-IGZO FETs into analog LSIs such as image sensors.

2. Experiments

Fig. 1 shows a STEM image of a submicron top-gate CAAC-IGZO FET. 45-nm-thick CAAC-IGZO is sputtered onto a base insulating film using a sputtering target whose chemical composition is In:Ga:Zn = 1:1:1. The equivalent oxide thickness of the gate insulator film in the CAAC-IGZO FET is 18.5 nm.

The 1/f noise is measured in a dark environment using an Agilent E4725A measurement system and a Cascade Microtech SUMMIT 11000B-M prober with temperature regulation (213 to 473 K). The 1/f noise in submicron CAAC-IGZO FETs with channel lengths $L = 0.35, 0.45, 0.5, 0.8 \mu m$ and a channel width $W = 10 \mu m$, and, for comparison, that in MOS (Si) FETs fabricated by 0.18 µm standard CMOS logic process are measured. For all measurements, the drain voltage $V_D$ is set to 50 mV. Fig. 2 shows the static $I-V$ characteristics of the CAAC-IGZO FETs for $L = 0.35$ and $0.8 \mu m$.

3. Results and Discussion

Fig. 3 shows the measured drain current noise spectral density ($S_{1f}$) of a CAAC-IGZO FET with $L = 0.35 \mu m$, $W = 10 \mu m$, and drain current $I_D = 1 \mu A$ (and also included are the analogous results for NMOS (Si) and PMOS (Si) FETs). Although we cannot quantitatively evaluate noise because of the different gate bias conditions for the FETs, the noise in the CAAC-IGZO FET tends to be lower than that in the NMOS (Si) FET.

Figs. 4 to 6 show $S_{1f}$ for CAAC-IGZO FETs with $L = 0.35, 0.45, 0.5, 0.8 \mu m$, $I_D = 1.06, 4.10, 8.07 \mu A$, and at temperatures of 223, 298, and 373 K. Unlike the NMOS (Si) FET, the CAAC-IGZO FET does not deviate from the straight 1/f noise for any condition. Such a deviation (bumps) in the NMOS (Si) FET could be caused primarily by random telegraph signal noise resulting from carrier generation and recombination (GR) [9]. CAAC-IGZO is a wide bandgap material (> 3.0 eV), its valence band maximum is flat, and its effective hole masses are much heavy [10]. Thus, carrier GR is hardly caused in CAAC-IGZO FETs. This is a great advantage of applying CAAC-IGZO FETs to analog LSIs.

Figs. 7 and 8 show normalized drain-current noise spectral density ($S_{1f}/I_D^2$) at 30 Hz as a function of gate overdrive voltage ($V_{gs} - V_{th}$) in NMOS (Si), PMOS (Si), and CAAC-IGZO FETs with $L = 0.35 \mu m$, and CAAC-IGZO FETs with $L = 0.35, 0.45, 0.5, 0.8 \mu m$. The NMOS (Si) FET, as $S_{1f}/I_D^2$ tends to be proportional to $(V_{gs} - V_{th})^2$, is described by a carrier number fluctuation ($\Delta N$) model [7], whereas, the PMOS (Si) FET and the CAAC-IGZO FET, as $S_{1f}/I_D^2$ tend to be proportional to $(V_{gs} - V_{th})^{3/2}$, are described by a mobility fluctuation ($\Delta \mu$) model [7]. This conclusion is supported by a previous report that used the $\Delta \mu$ model for a 20-µm IGZO FET [6]. In other words, the 1/f noise in the CAAC-IGZO FET comes from carrier scattering, with very little fluctuations in carrier number (i.e., GR is negligible).

Fig. 9 represents the relationship between $I_D$ and Hooge’s parameter $\alpha_H$ [6, 7], which is calculated from $S_{1f}/I_D^2$ at 30 Hz. The $\Delta \mu$ model is justified in the $I_D$ range where $\alpha_H$ is plateau [7]. $\alpha_H$ of a 0.8-µm CAAC-IGZO FET is approximately $9 \times 10^{-5}$ and $\alpha_H$ of a 0.35-µm CAAC-IGZO FET is
approximately $7 \times 10^{-5}$.  

Fig. 10 shows $S_{id}/I_d^2$ at 30 Hz and $I_d = 1 \mu A$ as a function of temperature. For the CAAC-IGZO FET, $S_{id}/I_d^2$ depends only weakly on temperature within the measured temperature range than that of the NMOS (Si) FET, though $S_{id}/I_d^2$ tends to decrease at high temperature.  

Fig. 11 shows the relationship between $I_d$ and the $S_{id}/I_d^2$ activation energy estimated by applying the Arrhenius equation to the temperature dependence of $S_{id}/I_d^2$ (as in Fig. 10) for various $I_d$. The activation energy falls within the range of approximately 40 to 70 meV. 

Fig. 12 shows temperature dependence of $\mu_{FE}$ of the PMOS (Si) FET and that of the CAAC-IGZO FET. For the CAAC-IGZO FET, $\mu_{FE}$ increases at high temperature, therefore, $S_{id}/I_d^2$ shows a negative correlation to $\mu_{FE}$. On the other hand, for the PMOS (Si) FET, $\mu_{FE}$ decreases at high temperatures. This result indicates that $\mu_{FE}$ of the CAAC-IGZO FET is determined by scattering that is different from lattice scattering, which determines $\mu_{FE}$ of the PMOS (Si) FET. On the basis of the Arrhenius equation, the activation energy $E_a$ of $\mu_{FE}$ of the CAAC-IGZO FET is estimated at approximately 30 meV, which is substantially consistent with the activation energy estimated from $S_{id}/I_d^2$ on above. This result indicates that conduction electrons scatter in the CAAC-IGZO FET from an energy barrier of the activation energy.

References