

Modeling of Nonlinear Thermal Resistance in FinFET

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Abstract—In this paper, self-consistent 3-D device simulations for exact analysis of thermal transport in FinFETs are performed. We analyze the temperature rise in FinFET devices with the variation in the number of fins (N_{fin}) and fin pitch (F_{pitch}). We investigate and formulate the nonlinear dependency of thermal resistance (R_{th}) on N_{fin} and F_{pitch} variation. The proposed formulation is implemented in industry standard BSIM-CMG model and validated with both experimental data and TCAD simulations.

I. INTRODUCTION

So far, lot of study and models have been proposed on self-heating [1–4] but some of these models [1, 2] are not based on proper thermal boundary conditions and realistic back end of line (BEOL). While other models [3, 4] are proposed based on single fin FinFETs, in which the additional rise of temperature in fins far away from the heat sink is not taken into account. In this work, we have done the calibrated 3D electro-thermal device simulations. Generally thermal resistance (R_{th}) is considered as inversely proportional to the number of fins (N_{fin}) in compact models. From our simulations we observe that R_{th} is not exactly inversely proportional to the N_{fin} and fin pitch (F_{pitch}). So we have proposed a updated model which captures accurate behavior of R_{th} with N_{fin} and F_{pitch} variation. This model is then included in the BSIM-CMG model.

II. CALIBRATION OF TCAD DEVICE

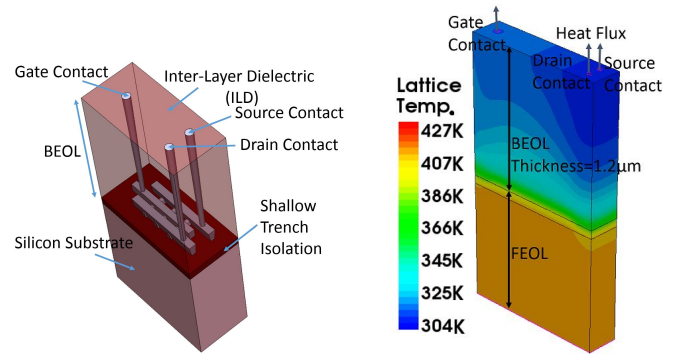
We used the TCAD Sentaurus for our simulations where we have simulated a well calibrated 3D bulk NMOS FinFETs having 1, 3, 5, 7, 9 and 11 fins as shown in Fig. 1(a).

Fig. 2 shows the calibration of our simulated device with the experimental data [5]. Exact matching of the experimental data with the simulated data reveals the accuracy of the models and their parameters used in these simulations.

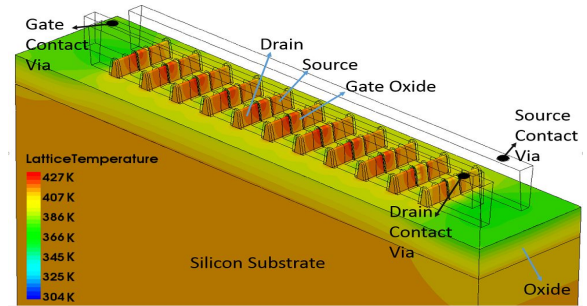
III. THERMAL BEHAVIOR AND ITS MODELING

A. N_{fin} variation

The temperature distribution across the BEOL and the substrate is shown in Fig. 1(b). From this figure, it is clear that the contribution of heat flux is through metal interconnects rather than the silicon substrate [3]. The fins in the middle region are hotter than the fins near the metal contacts as shown in Fig. 1(c). This is because of poor thermal coupling



(a) Bulk NMOS FinFET structure having 3 fins : 3D View. (b) Temperature distribution across seven metal layer interconnects of BEOL in FinFET device having 11 fins.



(c) Temperature distribution across the 11 fins in the FinFET. Fins in the middle region are hotter than the fins near the gate, source and drain contacts. Figure 1: Bulk NMOS FinFET structure using Sentaurus Technology Computer Aided Design (TCAD) Tools.

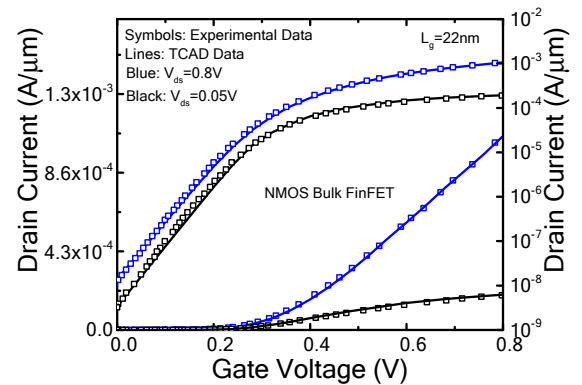


Figure 2: Calibration of TCAD models for drift diffusion transport with experimental data of FinFET with channel length of 22nm. Symbols: Experimental Data [5], Lines: TCAD Data. Bias conditions are: $V_{ds} = 0.05V$ and $0.8V$.

between the middle fin and the heat sink (metal contact vias). So temperature in the device increases with the number of fins as shown in Fig. 3, which results in the increase of thermal resistance than expected by the earlier models. This non-linearity in R_{th} with N_{fin} variation is captured by the α parameter. This study shows that thermal resistance should scale as $1/N_{fin}^\alpha$.

B. F_{pitch} variation

The decrease of F_{pitch} in the device causes crowding of heat which rises the device temperature resulting in higher R_{th} . The increase of F_{pitch} improves the thermal coupling between the fin and surrounding substrate, inter-layer dielectric, which decreases the device temperature results in lower R_{th} . Fig. 4 shows the maximum temperature profile in the device having seven fins with the F_{pitch} variation. To capture the effect of thermal resistance variation with F_{pitch} , we used β parameter. W_{th0} parameter is used to capture the width dependence.

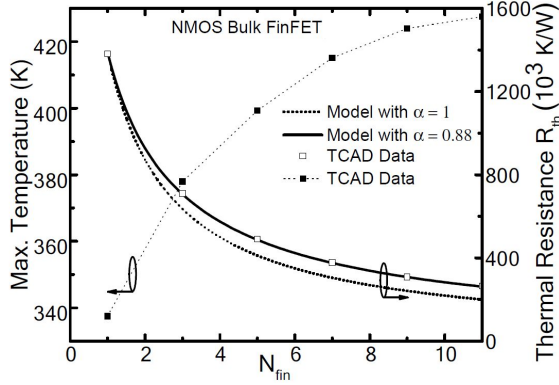


Figure 3: Maximum Temperature in the devices having various number of fins is plotted in the left axis. This rise in temperature with number of fins results in the increase of R_{th} which is plotted on right axis. Bias conditions are: $V_{gs} = V_{ds} = 0.8V$.

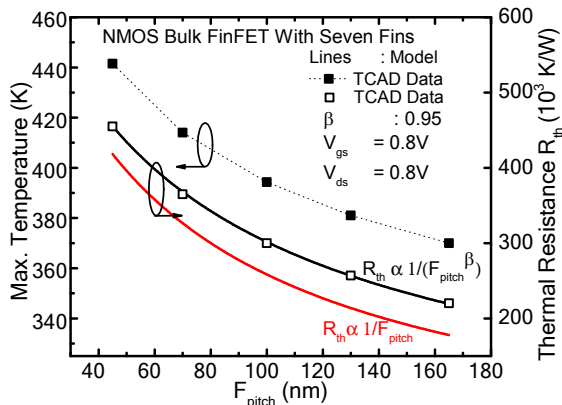


Figure 4: Maximum Temperature in the devices with F_{pitch} variation is plotted in the left axis. Thermal resistance and its model with F_{pitch} variation is plotted in the right axis. Parameter β is used to model R_{th} . Bias conditions are: $V_{gs} = V_{ds} = 0.8V$.

The model proposed for R_{th} is

$$R_{th} = \frac{R_{th0}}{W_{th0} + N_{fin}^\alpha * F_{pitch}^\beta}$$

This model is validated on TCAD data as shown in Fig. 3 and 4.

IV. BSIM-CMG MODEL CALIBRATION

We have the experimental data of FinFETs having channel length=100nm, fin width=50nm, fin height=40nm, EOT=1.2nm and Number of fins=2 and 20. We have validated the updated BSIM-CMG model against the experimental data. Drain current I_{ds} vs drain voltage V_{ds} and output conductance g_{ds} vs drain voltage V_{ds} for 2 and 20 fins are shown in Fig. 5. For this short channel device, the agreement of model with the experimental data shows that the model incorporated short channel and self heating effects correctly. From the Fig. 5, I_{ds} and g_{ds} of the model with and without self heating effects shows that self heating effects are more pronounced for 20 fin device than 2 fin device which clearly depicts the importance of α parameter in the model.

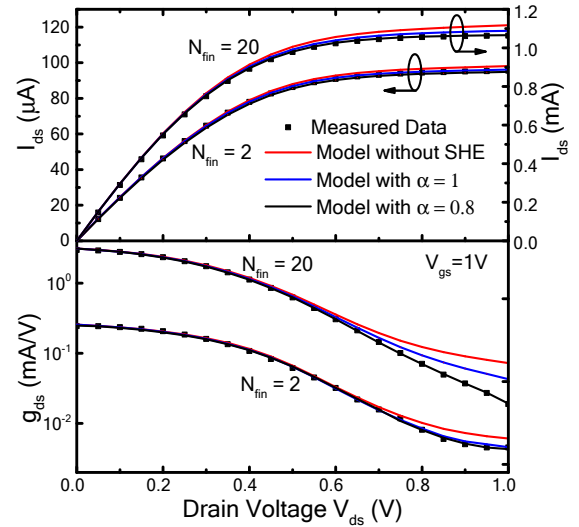


Figure 5: Drain current vs drain voltage and output conductance vs drain voltage curves for 2 and 20 fin FinFET devices with channel length = 100nm are calibrated by BSIM-CMG model with and without self-heating effects and shown in top and bottom figures respectively.

V. CONCLUSION

A new empirical model for nonlinear thermal resistance scaling with number of fins and fin pitch has been proposed and validated with the experimental data for FinFETs.

ACKNOWLEDGMENT

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