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Reliability of Improved CAAC-IGZO FET satisfying NOSRAM performance

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Abstract

A c-axis aligned crystalline indium-gallium–zinc-oxide (CAAC-IGZO) field effect transistor (FET) has a feature of low off-state leakage current. We have prototyped a non-volatile oxide semiconductor random access memory (NOSRAM) as an application of the CAAC-IGZO FET to a memory device. The reliability of the CAAC-IGZO FET is important for a stable operation of the NOSRAM. In this report, we have improved the CAAC-IGZO FET, and a buried-channel-type FET having a layered structure has been formed. By employing the buried-channel-type, we have succeeded in fabricating a CAAC-IGZO FET which satisfies the actual operation of the NOSRAM.

1. Introduction

C-axis aligned crystalline indium-gallium-zinc-oxide (CAAC-IGZO) is an oxide semiconductor with c-axis-aligned crystallinity. A CAAC-IGZO field effect transistor (FET) including the CAAC-IGZO in its active layer has extremely low off-state leakage current, and therefore, the application of the CAAC-IGZO FET to memory devices has been proposed [1–3]. We have previously proposed and prototyped a non-volatile oxide semiconductor random access memory (NOSRAM) as a memory device including the CAAC-IGZO FET with low off-state leakage current [4].

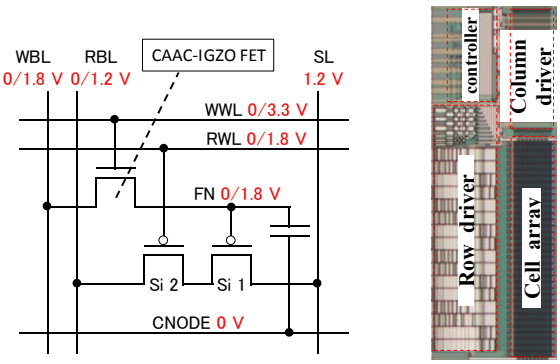
The NOSRAM functions as a non-volatile memory only by an on/off operation of the IGZO FET. However, at the time of driving the NOSRAM, a bias stress is applied to the IGZO FET. This bias stress is one factor of changing the characteristics of the IGZO FET, and the instability of the IGZO FET leads to abnormalities in writing and data retention and becomes a serious problem. The stability of the IGZO FET is very important.

In this report, we have improved the CAAC-IGZO FET to ensure its stability, and a buried-channel-type FET having a layered structure has been formed. By employing the buried-channel-type, we have succeeded in fabricating a reliable CAAC-IGZO FET which satisfies the actual operation of the NOSRAM.

2. Design of NOSRAM

We designed and prototyped a 1-kbit NOSRAM module. Fig. 1 shows the cell circuit, and Table I shows the operation specifications. Data can be rewritten with an on/off operation using the CAAC-IGZO FET. Electric charges are taken into or out of a floating node (FN) through a word bit line (WBL), so that data can be rewritten with an on/off operation. With characteristics of an CAAC-IGZO FET having extremely low off-state leakage current, the electric charges in the FN can be held only by turning off the CAAC-IGZO FET.

Fig. 2 shows I_d-V_g characteristics of our fabricated CAAC-IGZO FETs. The CAAC-IGZO FET is designed with a 180-nm channel length L. Normally-off characteristics and sufficient off-state characteristics are obtained from these FETs.



(a) 1-bit memory cell (b) Micrograph image

Fig. 1 Cell circuit of NOSRAM

Table I Specifications

NOSRAM	Technology	CAAC-IGZO FET	0.18 μm
		Si FET	0.18 μm
	Voltage	CAAC-IGZO FET	3.3 V
		Si FET	1.8 V/1.2 V
	Module area		1.1×0.5 mm^2
	Cell area		8.0×8.2 mm^2
	Capacitance		20.6 fF
	Number of bits		1040 bit

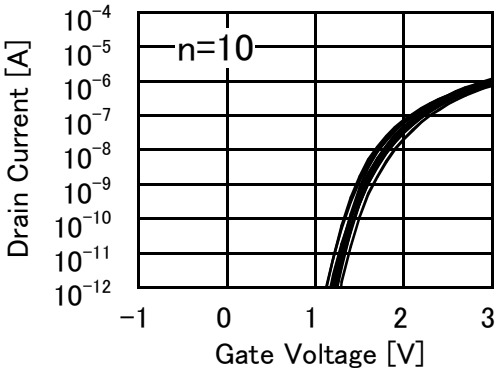


Fig. 2 I_d-V_g characteristics of fabricated CAAC-IGZO FETs

3. Improvement of CAAC-IGZO FET's reliability

A Few have reported the reliability of miniaturized CAAC-IGZO FETs[5]. For the purpose of improving the FET's reliability, an IGZO film with a layered structure was formed so that a buried channel was made as shown in Fig. 3. The IGZO film consists of three IGZO layers formed of materials having different band gaps, and the layer where a current flows is buried (Fig. 4). With this buried channel, the area where current flows can be controlled. And the capture of electric charges in trap states at the interface with the gate insulator or the base layer, which might cause reliability degradation, can be prevented.

The stress applied to the CAAC-IGZO FET in the NOSRAM under actual operation can be simulated using two kinds of bias temperature (BT) stresses. One is positive gate-bias temperature (+GBT) stress applied in rewriting, and the other is positive drain-bias temperature (+DBT) stress applied at the time of retention. In actual operation, the required lifetime under +DBT stress at the retention is overwhelmingly longer, and the reliability under +DBT stress is crucial.

Fig. 5 shows results of +GBT stress test on FETs with/without buried channels. The buried channel produced a difference in reliability in the results of +GBT stress test. The results revealed that the buried channel formed in the IGZO film with the layered structure can, as we assumed, improve +GBT resistance, that is, resistance against rewriting stress. On the lifetime that ΔV_{sh} is 0.1 V, the FETs with the buried channels can withstand more than 10^{11} cycles of stress tests even at 150°C and have enough reliability for actual rewriting operation. V_{sh} is defined as the gate voltage at a drain current of 1E-12 [A].

Figs. 6 and 7 show results of +DBT stress test on the buried-channel-type FETs. This +DBT stress test was carried out at 150°C for 300 h. ΔV_{sh} was suppressed to be lower than 0.1 V and the FETs showed favorable reliability. Since the stress at 150°C for 300 h can be converted into the stress at 85°C for 10 years, the FETs have enough reliability for practical usage.

4. Conclusion

NOSRAM is a memory device using a CAAC-IGZO FET, and the CAAC-IGZO FET was evaluated under a BT stress test in which the operation of the CAAC-IGZO FET was simulated. We have found that the CAAC-IGZO FET has high reliability by having a layered structure with a buried channel. Thus, we have succeeded in fabricating a CAAC-IGZO FET which satisfies the actual operation of the NOSRAM.

References

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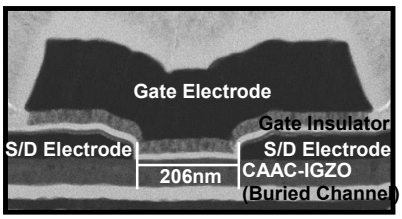

Fig. 3 Cross section of CAAC-IGZO FET in the *L* direction

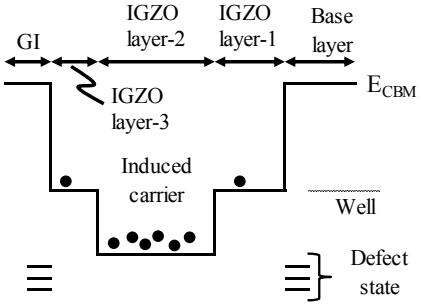

Fig. 4 Band model of buried channel.

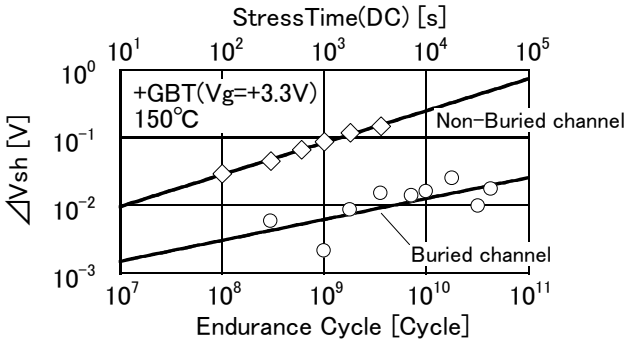

Fig. 5 Results of +GBT stress test.
corresponding to rewriting

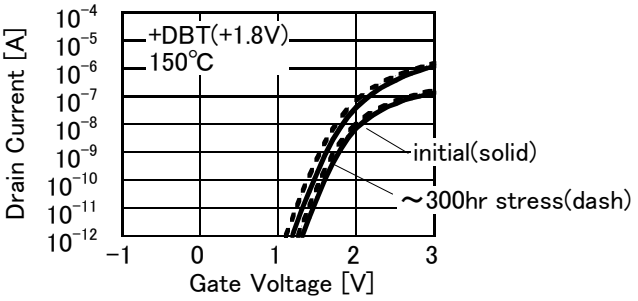

Fig. 6 Results of +DBTstress test (I_d-V_g curve).
corresponding to retention

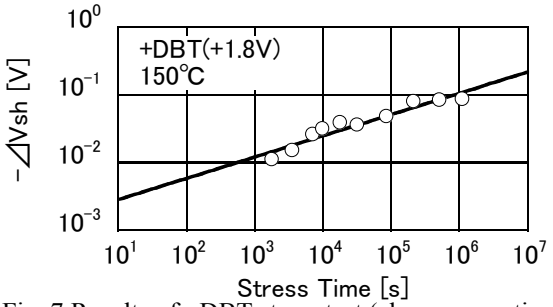

Fig. 7 Results of +DBT stress test (change over time).
corresponding to retention