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InGaAs channel for low supply voltage

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Abstract

We report our recent progress of InGaAs MOSFETs to obtain sufficient carrier supply by heavily doped source and good MIS quality with low effective oxide thickness. Simulation and experiments for InGaAs tunneling FETs (T-FETs) with heterojunction source are also reported for lower off-current.

1. Introduction

To obtain high performance in MOSFETs at low supply voltage, the introduction of high-mobility channel material is a promising approach. High mobility channel by InGaAs for nMOSFETs provides high current due to low channel resistance and high speed logic operation at low supply voltage [1,2]. However, introduction of InGaAs channel requires many studies, such as sufficient carrier supply from source and good MIS interface qualities. Moreover, simple high mobility channel is insufficient for low off-current, although recent circuits require low stand-by power in logic applications

In this report, sufficient carrier supply by heavily doped source [3,4] and good MIS quality [5] with low effective oxide thickness (EOT) are presented. Moreover, InGaAs tunneling FETs (T-FETs) with heterojunction source are also reported [6].

2. Heavily doped source

Doping concentration by ion implantation in InGaAs is limited to $1.4x10^{19}cm^{-3}$ by thermal annealing for activation [7]. To obtain higher carrier concentration for preventing source starvation [8], the epitaxial grown source is required. Thus, InGaAs regrown sources by selective regrowth were reported [9-12].

On the other hand, when we use an n-InP source, a structure similar to the structure with regrown source can be fabricated by using single epitaxial growth and InP selective etching[3]. Anisotropic selective etching was used for InP etching, and the crystallographic surface's gradient shorten the channel length (L_{CH}). Fig. 1 shows the I–V characteristics of a 50-nm-long channel InGaAs MOSFET with the InP source. The devices comprised 12- nm-thick InGaAs channel and a 10-nm-thick Al_2O_3 insulator. The current density of I_D = 2.4 mA/μm was observed at V_D = 0.5 V.

When the L_{CH} is shortened, it is expected that the device characteristics will improve. However, the further L_{CH} shrinkage was difficult due to proximity effect in the electron beam lithography (EBL). By using proximity effect correction (PEC) in EBL, we fabricated a 13-nm channel length InGaAs-MOSFET [4]. The devices comprised 9-nm-thick-$In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ composite-channel and a 5-nm-thick Al_2O_3 gate insulator. When L_{CH} was 13 nm, I_D of 2.14 A/mm at V_D of 0.5 V and V_G of 1.5V was obtained. Fig. 2 shows the maximum I_D at the V_D of 0.5 V as a function of L_{CH}. I_D increases as the L_{CH} becomes shorter. Estimated on resistance (R_{ON}) changes linearly with the L_{CH}, and Ron = 1.33 × L_{CH} + 205 [Ω μm] was obtained by the linear approximation. The I_D at the V_D of 0.5 V calculated from the approximate equation is also plotted in Fig. 2. This suggests that the maximum I_D saturation in the short channel region results from the S/D resistance (R_{SD}).

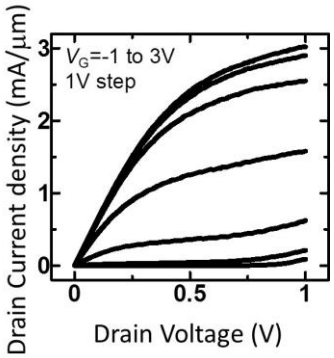

Fig. 1 I–V characteristics of a MOSFET with a heavily doped InP source [3].

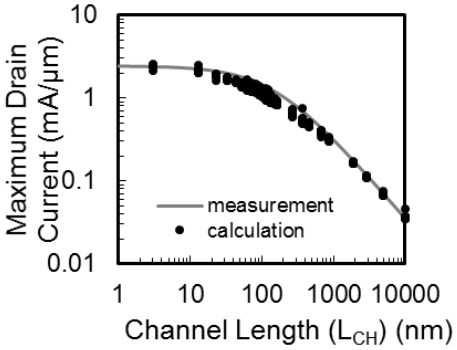

Fig. 2 L_{CH} dependence of the maximum drain current. Dot) measurement, line) calculation from approximate R_{ON} equation [4].

3. MIS characteristics

To obtain good drivability by gate bias or good subthreshold slope, good interface quality between InGaAs channel and gate insulator with low EOT is essential. When

native oxide is eliminated by using nitrogen plasma/TMA at $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface, we could get good interface properties. Prior to Al_2O_3 deposition, the samples were exposed to the *in-situ* nitrogen plasma and TMA cleaning. 2-cycles Al_2O_3 and 35-cycles HfO_2 were successively deposited at 300 °C. After metallization, the MOS capacitor was annealed at 350°C in H_2 for 90 sec. Measured EOT from C-V measurement was 0.74 nm. Fig.3 is interface trap density (D_{it}) dependence on the energy. Minimum D_{it} of sample after H_2 annealing is 1.3×10^{12} eV $^{-1}$cm^{-2} at -3.8 eV. To our knowledge, this is the lowest D_{it} value of $HfO_2/Al_2O_3/In_{0.53}Ga_{0.47}As$ gate stack with N_2 plasma cleaning method [13].

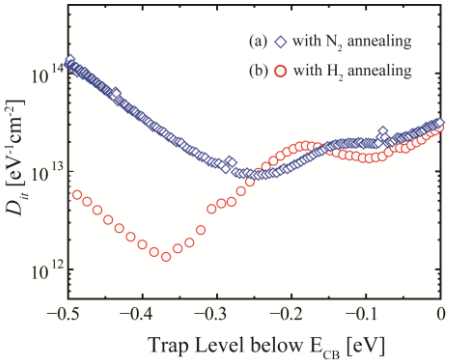

Fig. 3. D_{it} distribution of $HfO_2/Al_2O_3/In_{0.43}Ga_{0.57}As$ MOS capacitor [5]

4. T-FET by InGaAs/GaAsSb heterojunction

To obtain low off-current such as 10 pA/μm, we must introduce the mechanism to obtain steeper slope in subthreshold region than thermal limit. Most promising candidate is T-FET [14]. However, realizing high on-current in T-FETs is difficult due to tunnel resistance. In comparison to Si, narrow bandgap and small effective mass of InGaAs is useful in achieving smaller tunnel resistance and hence it stands as an attractive alternative. However, simple change of channel material is not sufficient. Thus we fabricated [6] a vertical FET with InGaAs/GaAsSb type-II heterojunction [15]. To obtain high on-current and low off-current simultaneously at low supply voltage, doping level of source and drain are important [6]. Fig. 4 shows calculated transfer characteristics of T-FETs when source carrier concentration was changed. In this simulation, it was assumed that InGaAs channel length is 40 nm, EOT is 1 nm, body width is 10 nm, drain bias is 0.5 V and n-InGaAs source carrier concentration is 1 x 10^{19}cm^{-3}. By increase of source carrier concentration, large access resistance or carrier starvation can be suppressed. However, the off-current increases. Similar tendency is observed when we change the carrier concentration of drain. If we assume V_G at I_{OFF} = I_D = 10 pA/μm as V_{OFF} and on-current is defined as I_D at V_G = V_{OFF} + 0.5 V, then simulated highest on-current is 466 μA/mm.

To confirm estimated characteristics, we have fabricated T-FET with heterojunction. At present, device with 26 nm wide mesa was fabricated and body width dependence of subthreshold slope was confirmed [6].

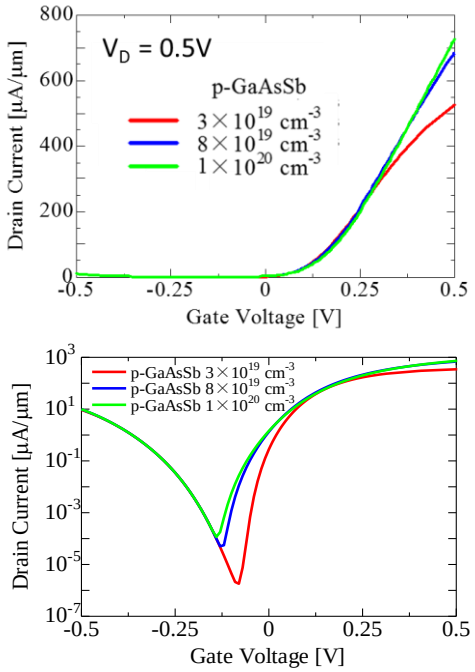

Fig. 4 Calculated transfer characteristics of T-FETs.

5. Conclusions

In InGaAs MOSFETs, 13-nm-devices are reported. In this region, drain current was limited by access resistance and lower contact resitance is essential for higher current. Good MIS characteristics of gate stack were also confirmed. Simulation of GaAsSb/InGaAs T-FETs shows good on-current and low off-current at low supply voltage simultaneously. We believe that combination of obtained results will result in high performance.

Acknowledgements

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References

[1] J. A. del Alamo Nature 479 (2011) 317
[2] M. Rodwell *et al.* IPRM Conf. Proc. (2007) 9.
[3] Y. Yonai, *et al.*, IEDM Tech. Dig. (2011) 307 .
[4] K. Ohsawa, *et al.* IPRM (2015) E.6.3.
[5] S. Netsu, *et al.* IPRM (2015) E.6.4.
[6] K. Ohashi, *et al.* Jpn. J. Appl.Phys. **54**, (2015) 04Df10.
[7] A. C. Lind *et al.* J. Vac. Sci. Technol., **B33** (2015) 021206.
[8] M. V. Fischetti, *et al.* IEDM Tech. Dig. (2007) 109.
[9] U. Singisetti, *et al.*, Phys. Status Solidi **C6** (2009) 1394.
[10] T. Kanazawa, *et al.*, Appl. Phys. Exp. **3** (2010) 094201.
[11] R. Terao, *et al.*, Appl. Phys. Exp. **4** (2011) 054201.
[12] M. Egard, *et al.*, IEDM Tech. Dig. (2011) 303.
[13] V. Chobpattana, *et al.* Appl. Phys. Lett., **102** (2013) 022907.
[14] A. C. Seabaugh and Q. Zhang, Proc. IEEE **98**, (2010) 2095.
[15] D. K. Mohata,et al., IEDM Tech. Dig. (2011), 781