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Evaluation of InAs HEMT with Non-alloyed Ohmic contacts & Mesa Sidewall Etch for RF and Low-power Logic Applications

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Abstract

An InAs HEMTs with Ti/Pt/Au non-alloyed ohmic contacts and mesa sidewall etch is successfully fabricated and evaluated for RF and low-power logic applications. The device exhibits a SS of 65.5 mV/decade with low DIBL of 22.2 mV/V and I_{ON}/I_{OFF} of 1.52 × 10^4 at V_{DS} = 0.5 V, and the off-state breakdown voltage was 6.6 V. For RF applications, the device shows a high f_T of 537 GHz and f_{max} of 486 GHz. These results demonstrate that mesa sidewall etch and non-an- nealed ohmic contacts can be applied to the fabrication of InAs HEMTs with excellent electrical characteristics.

1. Introduction

InP-based High electron mobility transistors (HEMTs) technologies are capable of providing high frequency application. However, conventional mesa isolation process causes sidewall leakage and results in increased gate leakage currents, subthreshold currents and lower breakdown voltage [1]. And using Au/Ge/Ni/Au ohmic metals could easily diffuse into adjacent semiconductor layers during annealing, which results in poor edge definition inadequate thermal stability [2]. In the previous study, researchers have acknowledged that sidewall leakage causes excessive gate leakage current, degraded breakdown voltage and non-alloyed ohmic contacts can provide good edge definition, smooth surface morphology.

In this study, a simple technique of sidewall etch and Ti/Pt/Au non-alloyed ohmic contacts was developed for RF and high speed application.

2. Device fabrication

The layer structure includes highly Si-doped, $In_{1-x}Ga_xAs$ cap layers, an InP etch stop layer, $In_{0.52}Al_{0.48}As$ barrier layer, a Si planar doping layer, a thin $In_{0.52}Al_{0.48}As$ spacer layer, and the $In_{0.65}Ga_{0.35}As$/InAs/$In_{0.65}Ga_{0.35}As$ layers to improve the electron transport properties [3][4]. The device fabrication process includes mesa isolation, ohmic metal deposition, silicon nitride passivation, gate recess, gate formation and Pt sinking process. The active area of the device was defined by wet etch using a H_3PO_4 base solution. After mesa definition, SA base solution was used for sidewall etch as shown in Fig. 1. Then, the non-annealing ohmic metal (Ti/Pt/Au) was deposited and the source, drain spacing was 3μm. The T-shaped gate was achieved using E-beam lithography. Finally, Schottky gate metal (Pt/Ti/Pt/Au) was deposited, the device was alloyed at 90^0C for Pt gate sinking. The low annealing temperature was used to avoid Pt diffusion into the channel layer owing to the thin barrier layer for the device.

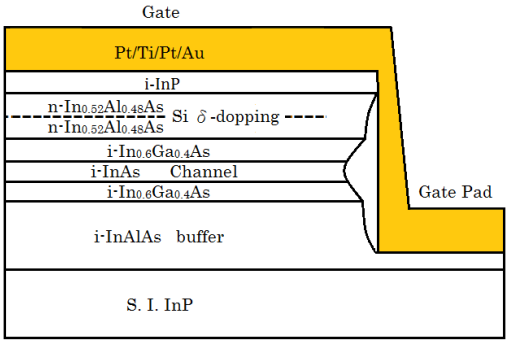

Fig. 1 The cross section of mesa sidewall etch.

3. Results and discussions

The InAs HEMTs with non-alloyed ohmic contacts and mesa sidewall etch obtains a high I_{ON}/I_{OFF} ratio, off-state breakdown voltage and low sub-threshold swing (SS) and drain induced barrier lowering (DIBL). Fig. 2 shows the DC characteristics of the device. It exhibits a maximum transconductance of 1508 mS/mm and the I_{DS} of 759 mA/mm were achieved at V_{DS}=1.0V and V_{GS}=0.5V as shown in Fig. 3. The InAs HEMTs was evaluated for high speed logic applications. Fig. 4 shows the sub-threshold characteristics of the device [5]. In a classic planar field-effect transistor with a long channel, the threshold voltage is independent of drain voltage bias. However, DIBL is a short-channel effect in devices, which is caused by gate shrinking and referring to the reduction of threshold voltage of the transistor at higher drain voltages. Because of using the non-alloyed ohmic contacts, lower DIBL value of 22.2mV/V was achieved. Also, excellent minimum SS of 65.5mV/decade was obtained at V_{DS} = 0.5 V, which

represents a fast switch transition. Besides, an I_{ON}/I_{OFF} of 1.52 x 10^4 was achieved. Fig. 5 shows the off-state breakdown voltage. Higher breakdown voltage of 6.6V was achieved by using sidewall etch as comparison with conventional mesa isolation [6]. Fig. 6 shows the frequency dependence of the current gain (H_{21}) and the power gain (MAG/MSG) for the device measured at V_{DS} = 1.2V. The values of intrinsic cut-off frequency and maximum oscillation frequency were extracted by extrapolating current gain and the power gain with a -20 dB/decade slope. A high intrinsic f_T of 537GHz and f_{max} of 486GHz were obtained for the device when device was biased at V_{DS}= 1.0V and V_{GS}= 0.16V. Excellent DC and RF characteristics of the device were achieved at low applied voltage of 1.2V.

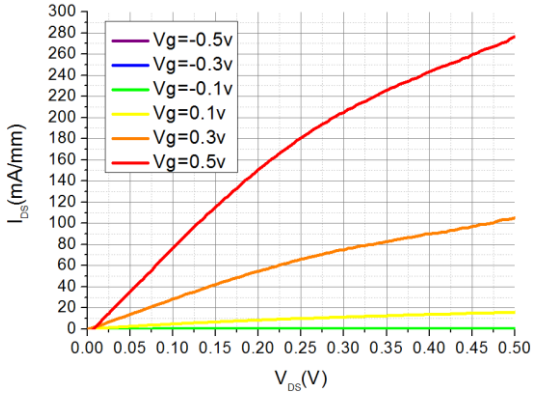

Fig. 2 DC characteristics for the InAs HEMTs with mesa sidewall etch and non-alloyed ohmic contacts. (I_{DS} versus V_{DS} curves)

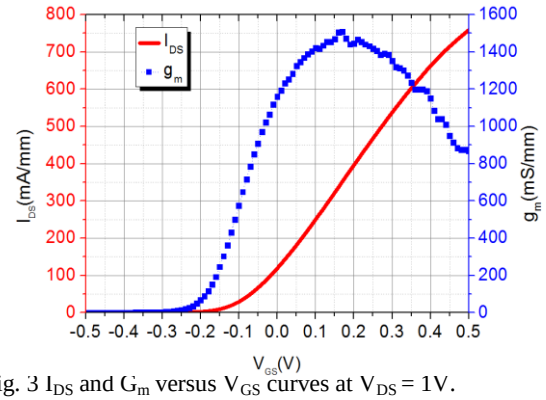

Fig. 3 I_{DS} and G_m versus V_{GS} curves at V_{DS} = 1V.

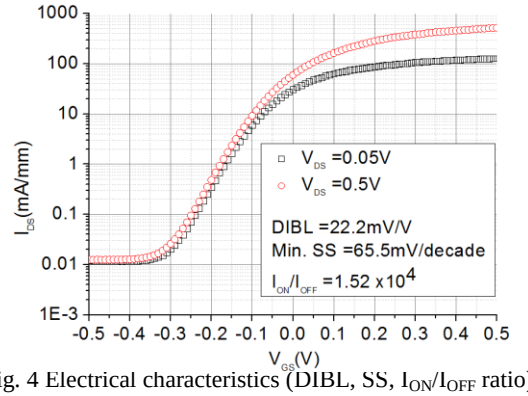

Fig. 4 Electrical characteristics (DIBL, SS, I_{ON}/I_{OFF} ratio)

4. Conclusions

In this study, InAs HEMTs Using mesa sidewall etch and non-alloyed ohmic contacts with a thin barrier layer design for logic and RF performance is demonstrated. Besides, with the Pt gate sinking process, the gate electrode becomes much closer to the channel layer, thus avoid short channel effect. The devices exhibit improved behaviors at low V_{DS} such as better current saturation (759 mA/mm), higher maximum transconductance ($g_{m,max}$ =1508 mS/mm). For logic applications, the device exhibited the DIBL of 22.2 mV/V, SS of 65.5 mV/decade, I_{ON}/I_{OFF} ratio > 10^4 and $BV_{off\text{-}state}$ of 6.6V. The device also shows RF performance with higher f_T (537GHz) and higher f_{max} (486GHz).

Overall, these experimental results demonstrate that InAs HEMTs with non-alloyed ohmic contacts and mesa sidewall etch has great potential for the next generation device for high-speed and low-voltage logic applications.

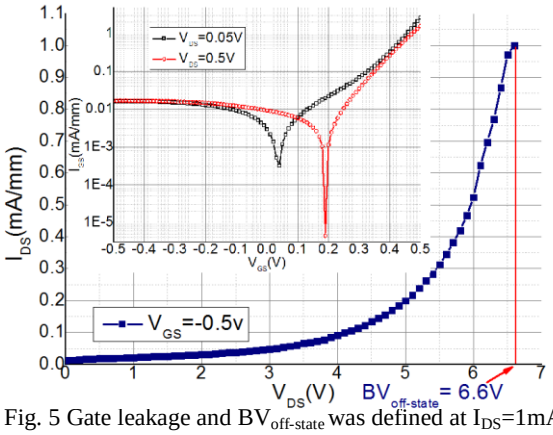

Fig. 5 Gate leakage and $BV_{off\text{-}state}$ was defined at I_{DS}=1mA/mm.

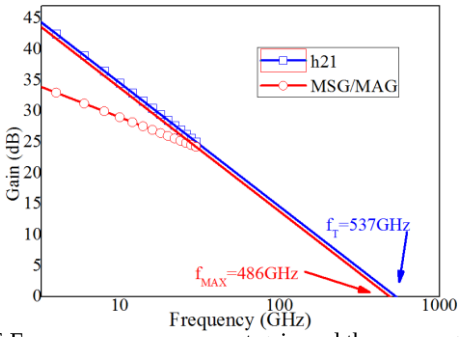

Fig. 6 Frequency versus current gain and the power gain .

Acknowledgements

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