Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp1034-1035

25nm InP HEMT TMIC Process with 1 THz Amplifier Circuit Gain

X. B. Mei, W. Yoshida, Z. Zhou, M. Lange, J. Lee, P. H. Liu, K. Leong, R. Lai, and W. R. Deal

Northrop Grumman Corporation
One Space Park Drive, Redondo Beach, CA 90278, USA
Phone: (310) 813-7499 E-mail: gerry.mei@ngc.com

Abstract

We report a 25nm InP HEMT which achieves 4 dB maximum available gain at 1 THz and a gain of 9 dB at 1 THz for a 10 stage circuit. This achievement is based on a new state-of-art transistor which demonstrates a peak cutoff frequency (f_T) of 725 GHz and an estimated maximum frequency of oscillation (f_{MAX}) of 1.5 THz.

1. Introduction

Rapid progress has been made in the realization of high frequency transistors and circuits. [1-7] Terahertz Monolithic Integrated Circuit (TMIC) compatible processes with a cutoff frequency (f_T) > 600GHz [1] and a maximum frequency of oscillation (f_{MAX}) approaching or exceeding 1 THz have been reported [1-5].

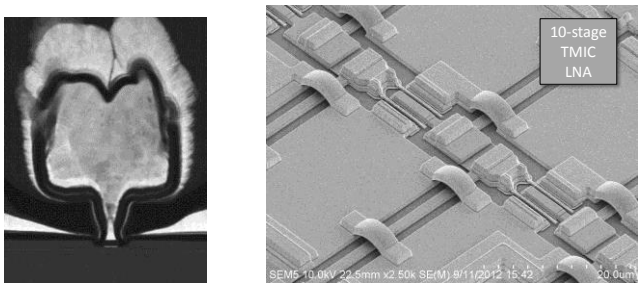
Our recent work has focused on scaling our InP HEMT process to 25 nm, which has further increased transistor and integrated circuit frequencies. TMIC amplifiers using this process have been reported at 0.67 THz [6] and 0.85 THz [7]. In this letter, we report on f_T and f_{MAX} capabilities of this recently developed 25 nm InP HEMT process. We also report achieving measured on-wafer circuit gain at 1.0 THz.

2. 25nm InP HEMT Process

Our TMIC process starts with epitaxial layers grown using Molecular Beam Epitaxy (MBE) on 3-inch semi-insulating InP wafers. Room temperature mobility of 13000 cm^2/Vs and an Ns of 4.0e12 cm^{-2} are typically obtained by Hall measurements.

The transistor was processed with a Ti/Pt/Au-based non-alloyed metal stack as the Ohmic contact and a source to drain distance at 0.5µm, only 0.1µm wider than the gate top which is 0.4µm. A contact resistance (Rc) of 40mΩ.mm and a source resistance as low as 140 mΩ.mm is demonstrated with this process.

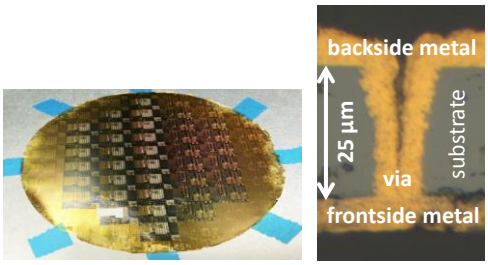
This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA). The views, opinions, and/or findings contained in this article/presentation are those of the author(s)/presenter(s) and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.



1a 1b

Fig. 1a. STEM image of the device gate cross-section. 1b. SEM image of TMIC.

The T-shaped 25nm gate pattern is defined using 100kV e-beam lithography (EBL). A gate recess is etched using a citric acid based solution. After the gate recess, a Ti/Pt/Au-based gate metal is evaporated with e-beam evaporation. Fig 1a shows a STEM image of the cross-section of a completed transistor gate. The rest of the TMIC process includes two layers of metal interconnection, thin film resistors with 20 Ω/sq and 100Ω /sq sheet resistivity and MIM capacitors with 600 pF/mm^2 sheet capacitance. The TMIC is fully passivated with SiN. The wafer then goes through the backside process which is critical for the TMIC performance. It is thinned to 25 µm for substrate mode suppression. Through-substrate vias are also etched and metalized to connect the frontside metal and the backside metal. A SEM image of the completed TMIC is shown in Fig. 1b. Fig. 2a shows a completed thin wafer and Fig. 2b shows a cross-section of a via and its metallization.



2a 2b

Fig. 2a. Image of a completed TMIC wafer with 25µm thickness. 2b. Cross-section of a through-substrate via.

3. Transistor characterization

The dc Electrical parameters are listed in Table 1. The device shows excellent pinch-off characteristics and controlled output conductance to Vds=1.0V. A peak transconductance (g_{mp}) of 3.0 S/mm is measured. An on-

state breakdown voltage($BV_{onstate}$) of 2.2V and off-state breakdown voltage ($BV_{offstate}$) of 3.0V is typical for this process.

Microwave measurements have been taken on a 1 to 110 GHz probe station on a two finger 30µm device biased at V_d = 0.8V and I_d = 600 mA/mm. This gives an f_T of 725GHz by extrapolating $|h_{21}|$ to unity with a -20dB/decade slope (Fig. 3). Shown in Fig. 4 is the MAG/MSG measured on a two finger 10µm device biased at V_d =1.2V and I_d =450mA/mm. The measurement was carried out for three different frequency bands, i.e. 20GHz-110GHz, 500GHz-700GHz and 750GHz-1.0THz, respectively. An f_{MAX}=1.5THz is estimated. 4 dB of maximum available gain is measured at 1.0 THz frequency, making this transistor capable of amplification at this frequency.

R_c	0.04 Ω.mm
R_s	0.14 Ω.mm
Gmp (V_d=1V)	3.0 S/mm
V_T (V_d=1V)	-0.1V
BV (off-state)	3.0V
BV (on-state)	2.2V
f_T	0.725 THz
f_{MAX}	1.5 THz

Table 1. Electrical parameters of a 25 nm transistor.

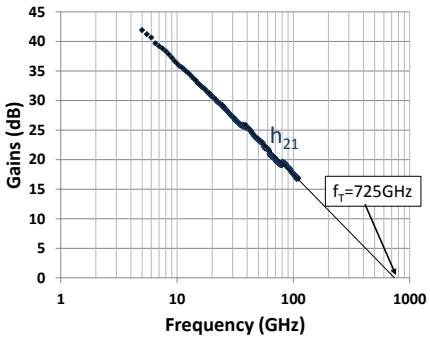


Fig. 3 The h_{21} of a 2-finger 30µm device biased at V_d=0.8V and I_d=600mA/mm showing an f_T=725 GHz.

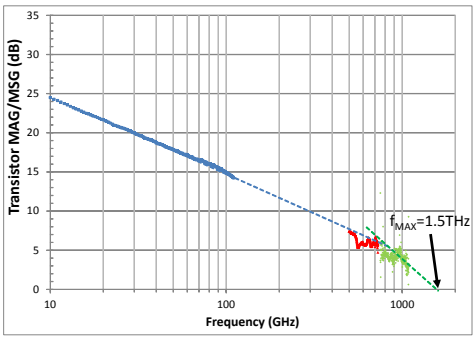


Fig. 4 The MAG/MSG of a 2-finger 10µm device biased at V_d=1.2V and I_d=400mA/mm.

4. TMIC amplifier Demonstration

A 10-stage amplifier circuit was designed with 8 µm transistors for each stage. The design is based on a grounded coplanar single-ended common source configuration. A picture of the completed circuit is provided in the inset of Fig.5.

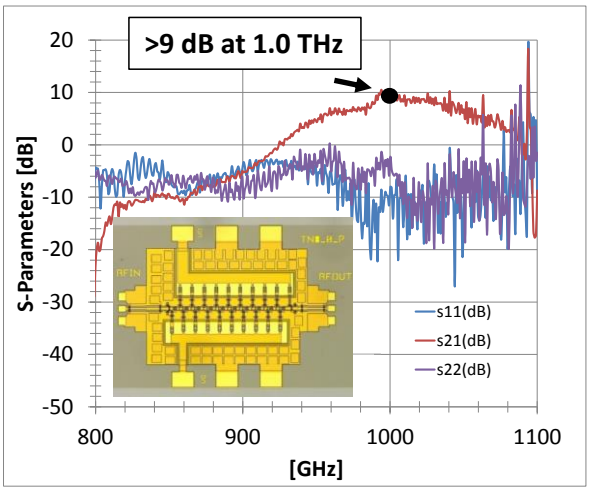


Fig. 5 On wafer measurement results showing 9 dB on-wafer gain at 1.0 THz.

The TMIC was measured on-wafer using a test set which consists of WR1.0 frequency extenders covering 750-1100 GHz interfaced with a Rohde and Schwarz Vector Network Analyzer. The measurement results are shown in Fig.5. 9 dB gain was measured at 1.0 THz, making this the first demonstration of transistor amplifier gain at and above the 1.0 THz mark.

Acknowledgements

The authors would like to thank Dr. Dev Palmer of DARPA, and Dr. Alfred Hung of ARL and to acknowledge NGAS contributors in microelectronics, machining, and testing groups.

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