Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp1046-1047

MOS Characteristics on Homoepitaxial GaN Layer

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Abstract

In this paper, we report the lateral MOSFETs on homoepitaxial p-GaN layer to investigate the MOS channel behavior. We evaluate the quality of the moderately-doped p-GaN layer and low interface state density on SiO_2/n-GaN MOS interface as the elemental parts for MOSFETs. The fabricated MOSFETs show reasonable V_{th} and field effect mobility.

1. Introduction

GaN is one of the promising materials for next generation power conversion systems and attracting much attention due to its wide bandgap energy and the large critical electric field [1]. AlGaN/GaN high electron-mobility transistors (HEMTs) have been developed extensively so far with heteroepitaxial GaN layer on sapphire or Si substrates. However, the vertical device structures with homoepitaxial GaN layer on GaN substrates are more suitable to handle high voltage and large current [2, 3], and also MOS-gate is preferable for switching devices because of its normally-off behavior.

There are many prior arts regarding the dielectric/GaN interface on heteroepitaxial GaN layers grown on sapphire or Si substrates, but there are few reports focused on the MOS channel characteristics on the homoepitaxial p-type GaN layer. Thanks to the recent developments of bulk GaN crystal growth, we are able to perform the investigation of GaN MOS characteristics based on the high quality homoepitaxial GaN layer. In this study, by using the homoepitaxially grown GaN, we investigate the characteristics of moderately-doped p-type GaN layer, and the SiO_2/GaN interface, which are the elemental parts of MOSFETs, and then demonstrate the lateral MOSFETs in order to evaluate the MOS channel characteristics on the homoepitaxial layer.

2. Experimental Procedure

Samples used in this study were fabricated on homoepitaxial GaN layers grown by MOCVD on free-standing n-type GaN (0001) substrates obtained by HVPE growth.

For characterization of moderately doped p-type GaN layer, 1-μm-thick Mg-doped p-type GaN layer with Mg impurity on the order of 10^{17} cm^{-3} were grown on the n-GaN/substrate. In addition, 100-nm-thick heavily-doped p-GaN layer was grown on it in order to achieve the good ohmic contacts. To carry out precise measurements, clover-leaf patterns were fabricated by photolithography and dry-etching. Note that the heavily-doped layer was removed by dry etching except the contact region where the ohmic metals were placed. Hall measurements were carried out in the wide temperature range of 120-873 K to perform reliable analysis.

Characterization of the MOS interface was performed on SiO_2/n-GaN capacitors. 100-nm-thick SiO_2 layer was deposited at 300-400°C on homoepitaxial n-GaN layer using a plasma-CVD apparatus developed by Univ. of Yamanashi and SST Inc. Aluminum layer was deposited to form circular metal patterns on the SiO_2 layer. Backside contact was also formed by Aluminum deposition to obtain the vertical MOS capacitor structure. *I-V*, *C-V*, and *G-V* measurements were carried out to evaluate the dielectric breakdown and the MOS interface state.

Lateral MOSFETs were fabricated on 2-μm-thick homoepitaxial p-GaN layer with Mg concentration of 5×10^{17} cm^{-3}. The source/drain regions were selectively formed by Si ion implantation followed by the activation annealing before the gate oxide deposition. Aluminum metal was used as the gate metal and also the source/drain contact metal to simplify the process. I_d-V_g and I_d-V_d characteristics were measured.

3. Results and Discussion

Evaluation of p-type GaN homoepitaxial layer

The temperature dependence of hole concentration and the mobility for the moderately-doped p-GaN layer is shown in Fig. 1. At around the maximum temperature, the saturation of hole concentration is observed, which gives accurate fitting results. The fitting is done by the semiconductor carrier statistics with the consideration of lowering of the activation energy by ionized acceptors [4]. The acceptor concentration (N_A), the compensating donor concentration (N_D), the activation energy (ΔE_A), and the hole effective mass (m^*/m_0) are extracted by the fitting. The results show that N_D is on the same order of the typical background donor level for unintentionally-doped n-GaN layers, indicating high quality p-GaN layer without any defect in-

troduced by Mg doping.

SiO_2/GaN MOS interface

Although SiO_2 is formed by a deposition method, the fabricated SiO_2/GaN MOS capacitors show good *I-V* characteristics exhibiting dielectric breakdown at around 9-10 MV/cm. *C-V* characteristics show negligible frequency dispersion as shown in Fig. 2, indicating very low interface trap density (D_{it}). We tried D_{it} analysis by a Hi-Lo method and a conductance method, but both give no apparent interface trap response. This suggests that we obtained high quality SiO_2/GaN interface with few interface state, which is estimated in the range of 10^{10} $cm^{-2}eV^{-1}$.

Lateral MOSFET

The typical I_d-V_g transfer characteristics of fabricated MOSFETs are shown in Fig. 3 (a). The threshold voltage (V_{th}) is defined as the gate bias intercept of the linear extrapolation of I_d, and V_{th} ~ 15 V is extracted, which is close to the simulated value of 18 V for MOSFETs consist of the p-type layer with N_A of 5×10^{17} cm^{-3} and 100-nm-thick SiO_2 gate oxide. Below V_{th}, the I_d shows gradual increase. The reason is under investigation but this might be due to the channel inhomogeneity caused by the process damage such as the post-implantation annealing, or the difference of the MOS interface quality between n-GaN surface and p-GaN surface. The I_d-V_d output characteristics show the text-book-like curves which exhibit increasing I_d spacing against V_g increase as shown in Fig. 3 (b).

The field effect mobility gradually increases by applying the gate voltage and shows the peak value of 29.7 cm^2/V-s. This value is not as high as the previous reports on heteroepitaxial p-GaN [5]. It may be due to the higher doping concentration of the p-GaN layer used in this study. We believe the MOS channel mobility will be improved by using lightly-doped p-GaN layer such as 1×10^{17} cm^{-3} or lower, which will be the future work.

4. Conclusion

We investigated the lateral MOSFETs and evaluated the elemental parts of them. The moderately-doped p-type GaN layer was characterized by Hall-effect measurement, and the low compensation ratio was confirmed. MOS interface quality was investigated by SiO_2/n-GaN MOS capacitor, and no obvious interface state was observed. The fabricated lateral MOSFETs exhibited reasonable V_{th} and the field effect mobility. Further doping control of high quality homoepitaxial p-GaN layer and evaluation of MOS channel characteristics on it are the future work.

Acknowledgements

This work was partly supported by Council for Science, Technology and Innovation (CSTI), Cross-ministerial Strategic Innovation Promotion Program (SIP), "Next-generation power electronics" (funding agency: NEDO).

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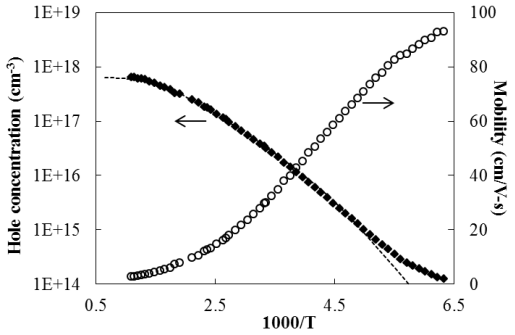

Fig. 1. Temperature dependence of hole concentration and mobility in a moderately-doped p-GaN layer obtained by Hall-effect measurement. $N_A = 6.5\times10^{17}$ cm^{-3}, $N_D = 7.5\times10^{15}$ cm^{-3}, $\Delta E_A = 243$ meV, and $m_h^*/m_0 = 2.0$ were extracted by the fitting (dashed line).

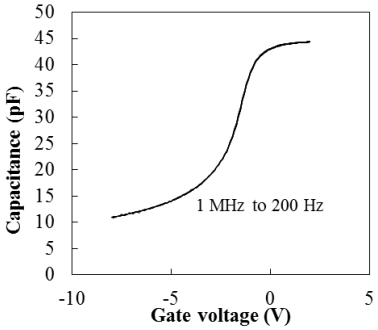

Fig. 2. Frequency dispersion of *C-V* curve measured on the SiO_2/n-GaN MOS capacitor.

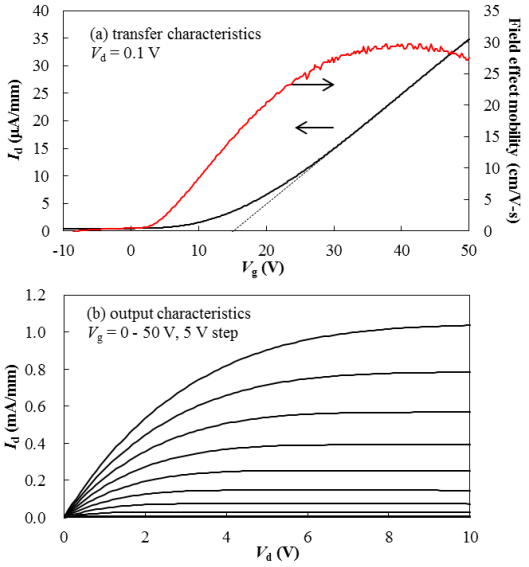

Fig. 3. (a) I_d-V_g transfer characteristics and (b) I_d-V_d output characteristics measured on MOSFET of W/L = 100/100 μm and d_{ox} = 100 nm.