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Fabrication and characterization of AlTiO/InAlN/AlN/GaN metal-insulator-semiconductor field-effect transistor

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Abstract — We fabricated AlTiO/InAlN/AlN/GaN metal-insulator-semiconductor field-effect transistors (MIS-FETs) with an AlTiO gate insulator obtained by atomic layer deposition. Characterization of the fabricated MIS-FETs shows good current drivability with high drain currents and transconductances, and low gate leakage currents in comparison with those of Schottky-FETs. We investigated the conduction mechanism of the gate leakage currents based on their temperature dependence.

1 Introduction

GaN-based field-effect transistors (FETs) have attracted much attention for their potential uses in high-frequency and high-power device applications. In particular, AlGaN-GaN metal-insulator-semiconductor FETs (MIS-FETs), having merits of gate leakage reduction and passivation effects, have been developed extensively. As a gate insulator, high-dielectric-constant (high-k) oxide materials, Al_2O_3 [1], HfO_2 [2], TiO_2 [3], and also high-k nitride materials, such as AlN [4, 5], BN [6], have been investigated. On the other hand, InAlN-GaN FETs using GaN-lattice-matched $In_{0.18}Al_{0.82}N$ as a barrier layer is highly anticipated owing to their high-density two-dimensional electron gas formed by the large spontaneous polarization [7]. For InAlN-GaN FETs, the adoption of MIS-FET structures, where a gate insulator is deposited on the InAlN layer, is also quite important. Although InAlN-GaN MIS-FETs using Al_2O_3 [8], HfO_2 [9], or ZrO_2 [9] as a gate insulator have been reported, there is still much room for developments of InAlN-GaN MIS-FETs, where choice and examination of gate insulators are critical issues. AlTiO, alloys of TiO_2 and Al_2O_3, is one of promising insulators [10, 11], because we can design physical properties between TiO_2 (dielectric constant $k \sim 60$, bandgap $E_g \sim 3$ eV) and Al_2O_3 ($k \sim 9$, $E_g \sim 7$ eV) by choosing its composition [12]. In this study, using AlTiO as a high-k gate insulator, we fabricated and characterized AlTiO/InAlN/AlN/GaN MIS-FETs.

2 Experiments and results

As a gate insulator, we employ Al_xTi_yO ($x : y = 0.73 : 0.27$) deposited by atomic-layer-deposition (ALD) using trimethylaluminum (TMA), tetrakis-dimethylamino titanium (TDMAT), and H_2O as precursors, based on the consideration of the trade-off between k and E_g, where we obtain $k \sim 13$, $E_g \sim 6$ eV, and the breakdown field $\sim$ 6.5 MV/cm. We fabricated AlTiO/InAlN/AlN/GaN MIS-FETs by the following processes. On $In_{0.18}Al_{0.82}N$(10 nm)/AlN(0.8 nm)/GaN heterostructure obtained by metal-organic vapor phase epitaxy on sapphire(0001), Ti/Al/Ti/Au Ohmic electrodes were formed and a 10-nm-thick AlTiO film as a gate insulator was deposited by ALD. After device isolation by B^+ implantation and formation of Ni/Au gate electrodes on the AlTiO layer, a post-gate-deposition annealing in Ar-H_2 completed the device fabrication. Also, we fabricated Schottky-FETs (S-FETs) without a gate-insulator for comparisons. The FETs have a gate length of 0.25 μm, a gate width of 50 μm, a gate-drain spacing of 3 μm, and a gate-source spacing of 2 μm. In Fig. 1, we show the output (top) and transfer (bottom) characteristics of the fabricated MIS-FETs and S-FETs, both exhibiting good current drivability with drain currents I_D of more than 1 A/mm, and a maximum transconductance $g_m \sim$ 180 mS/mm for the MIS-FETs and $\sim$ 240 mS/mm for the S-FETs. The insertion of the AlTiO gate insulator between the gate electrode and the InAlN slightly reduces the transconductances. Furthermore, owing to the good insulating properties of the AlTiO gate insulator, the gate current I_G of the MIS-FETs is reduced by about 4 orders of magnitude for both reverse and forward biases in comparison with those of the S-FETs.

In order to further examine the device operations, we carried out C-V measurements at frequency $f = 1$ MHz for Schottky and MIS capacitors with AlTiO thicknesses $d \simeq 10$ and 30 nm, having the 100 μm $\times$ 100 μm gate electrode surrounded by the Ohmic electrode. From C-V characteristics of the capacitors shown in Fig. 2(a) and n_s-V characteristics shown in Fig. 2(b), where n_s is obtained by integrating C, we can estimate the AlTiO dielectric constant $\simeq 14$ and InAlN/AlN average dielectric constant $\simeq 9.8$. From the C-V measurements results, parameters related to the band line-up are also extracted; we obtain $\phi - \varphi - \Delta E_c \simeq 1$ eV for the MIS devices and $\phi' - \Delta E_c \simeq 0.5$ eV for the Schottky devices, where ϕ and ϕ' are the Schottky barrier heights for Ni/AlTiO and Ni/InAlN, respectively, and φ and ΔE_c are the conduction band offsets for AlTiO/InAlN and InAlN-GaN, respectively. Thus, we conclude a relation $\phi - \varphi \simeq \phi' + 0.5$ eV, suggesting a vacuum level discontinuity of $\simeq 0.5$ eV at the Ni/InAlN interface. Applying the obtained dielectric constants and band line-up parameters for the MIS devices, we can calculate the electric field F in the AlTiO as a function of the gate voltage, which can be utilized to analyze the gate leakage current conduction mechanism.

Figure 3 (a) shows the current density (J) - voltage (V) characteristics of the MIS capacitor with $d \simeq 10$ nm for several temperatures. The leakage currents increase with increase in temperature. We also observe a signifi-

cant increase in the leakage currents for forward biases. Figure 3 (b) shows the Poole-Frenkel (PF) plot using the calculated electric field F for the forward biases. In the high-field region $F \gtrsim 1$ MV/cm, the gate leakage currents obey the PF conduction given by

$$J = CF\exp\left[-\frac{q}{k_{\rm B}T}\left(\phi_{\rm B}-\sqrt{\frac{qF}{\pi k\varepsilon_0}}\right)\right] \quad (1)$$

$$= F\exp\left[A(T)\sqrt{F}+B(T)\right], \quad (2)$$

where q is the electron charge, $k_{\rm B}$ is the Boltzmann constant, ε_0 is the vacuum dielectric constant, T is the temperature of the system, k is the effective dielectric constant in the PF conduction, $q\phi_{\rm B}$ is the trap depth, and C is the constant. Figure 3 (c) and (d) show the temperature dependences of $A(T)$ and $B(T)$ in Eq. (2), respectively. The former gives the effective AlTiO dielectric constant $k \sim 10$ in the PF conduction, while the latter gives the trap depth $q\phi_{\rm B} \sim 0.4$ eV in the AlTiO.

3 Summary

Using the AlTiO obtained by ALD as a high-k gate insulator, we fabricated and characterized AlTiO/InAlN/AlN/GaN MIS-FETs, exhibiting good current drivability with high drain currents and transconductances, and low gate leakage currents. We found that the gate leakage currents obey the PF conduction mechanism.

Acknowledgement

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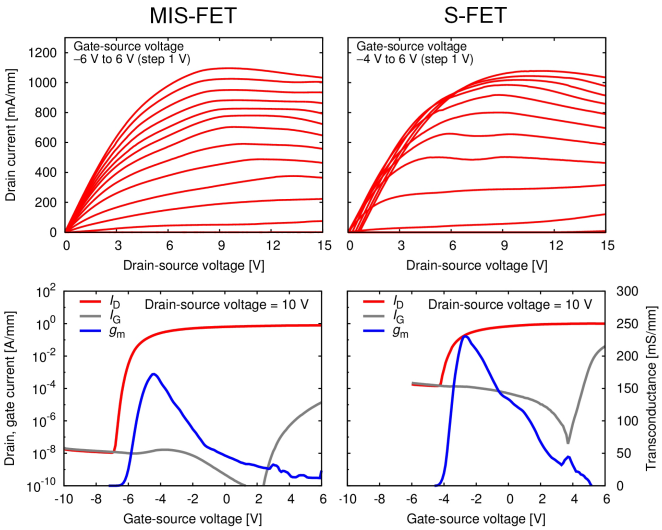

Fig. 1: Output (top) and transfer (bottom) characteristics of the fabricated MIS-FETs and S-FETs.

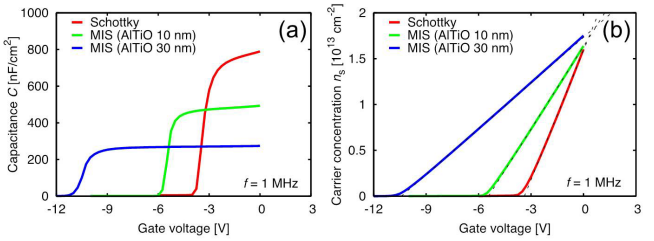

Fig. 2: (a) C-V characteristics and (b) $n_{\rm s}$-V characteristics of Schottky and MIS capacitors measured at frequency f = 1 MHz.

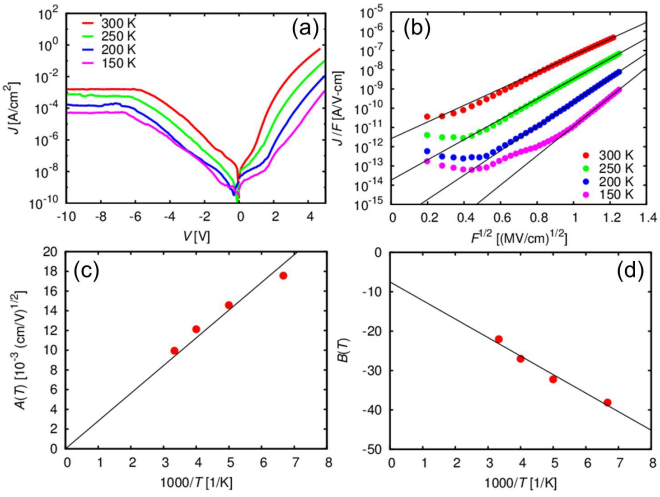

Fig. 3: (a) J-V characteristics and (b) PF plot of the MIS capacitor for several temperatures. Temperature-dependences of (c) $A(T)$ and (d) $B(T)$.