Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp1054-1055

Development of Novel 1200V-class 4H-SiC Implantation and Epitaxial Trench MOSFETs with Low On-resistance

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Abstract

This paper presents a newly developed 1200V-class 4H-SiC implantation and epitaxial trench metal-oxide-semiconductor field-effect transistor (IETMOSFET). It takes advantage of high quality p- and n-epitaxial layers for a channel and a trench current spreading layer (TCSL), respectively. They can enhance not only channel mobility, but also bulk mobility for the current spreading by avoiding damages and impurity variations caused by implantations. By optimizing the geometry of p-base regions under a gate trench structure, we have obtained a low specific on-resistance ($R_{ON}A$) of 1.8 mΩ cm^2 with a breakdown voltage (BV_{DSS}) above 1200 V.

1. Introduction

Silicon carbide (SiC) power devices are now employed in a variety of power systems, including power supplies, photovoltaic converters, air conditioners, and motor controls for elevators and railcars, because of their dramatic reduction of switching loss. Implantation and epitaxial MOSFETs (IEMOSFETs) have been developed, in which the channel mobility is enhanced by utilizing low doped p-type epitaxial layers to avoid implantation damages [1]. A trench SiC-MOSFET is expected to have low $R_{ON}A$ for its high cell density and high channel mobility on the trench sidewall [2]. However, high electric field is likely to be developed at the gate oxide and also the p-epitaxial layer for the channel. That may cause a critical issue of the gate oxide reliability and also punch-through of the low doped p-epitaxial layer with high channel mobility. Based on IEMOSFETs, we present a newly developed IETMOSFET protecting the bottom oxide and the low doped p-epitaxial layer for the channel.

2. Experimental

A schematic cross-section of an IETMOSFET fabricated on 4H-SiC (000-1) face is shown in Fig. 1. The first p-base (PBA1) regions were locally formed by multiple aluminum implantations with a depth of 0.5 µm and a concentration of 2×10^{18} cm^{-3} in the n$^-$-drift layer with a thickness of 10 µm and a doping concentration of 8×10^{15} cm^{-3}. Then a current spreading layer (CSL) was formed by multiple nitrogen implantations with a depth of 0.7 µm and a concentration of 1×10^{17} cm^{-3}. The TCSL with a thickness of 0.6 µm and a concentration of 5×10^{16} cm^{-3} was epitaxially grown on PBA1 and CSL regions. The 2nd p-base (PBA2) regions were locally formed by implantations of the same concentrations of PBA1 regions. A p-epitaxial layer with a thickness of 1.6 µm and a concentration of 0.1-1.0 × 10^{17} cm^{-3} was grown on TCSL and PBA2 regions. Gate trenches with a well-controlled shape were formed by reactive ion etching and annealed in hydrogen ambient [3]. A gate oxide film with a thickness of 100 nm was deposited and treated by hydrogen rich wet re-oxidation [4]. The following detailed fabrication processes were reported elsewhere [1]. We fabricated small transistors with 100 cells for optimization of the IETMOSFET structures with the cell pitch from 5.4 µm to 10.6 µm and large transistors of the chip size of 3 x 3 mm^2. I-V characteristics were measured on wafers.

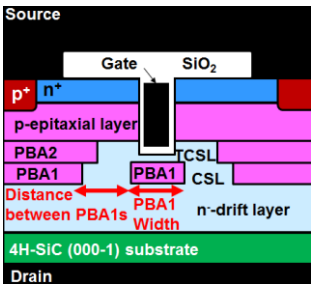


Fig. 1 A schematic cross-section of an IETMOSFET.

3. Results

Using Synopsys-TCAD (Sentaurus Device Simulator), the dependence of the maximum oxide electric field (E_{OX}) on PBA1 width at the distance of 1.3 µm between PBA1s was calculated as a function of drain voltage in Fig. 2. E_{OX} is well suppressed, when the PBA1 width is wider than the trench width of 1.0 µm.

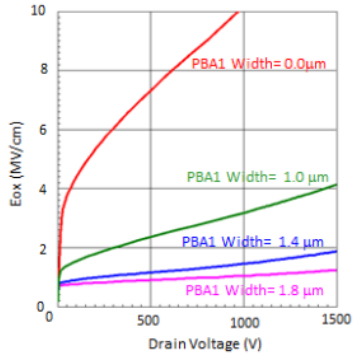


Fig. 2 Device simulation results of PBA1 width dependence of E_{OX} as a function of drain voltage.

*On a leave of absence from Sumitomo Electric Industries, Ltd.

Figure 3 shows the experimentally measured $R_{ON}A$ and BV_{DSS} depending on the PBA1 width. The PBA1 width should be more than the trench width of 1.0 µm to maintain the breakdown voltage, while $R_{ON}A$ does not change from 1.4 µm to 1.8 µm of PBA1 width, which means that the TCSLs effectively enhance the current spreading.

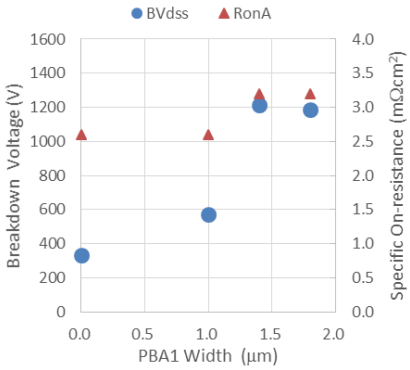


Fig. 3 $R_{ON}A$ and BV_{DSS} depending on the PBA1 width of IETMOSFETs with the cell pitch of 10.6 µm.

Figure 4 shows the experimentally measured $R_{ON}A$ and BV_{DSS} depending on the distance between PBA1s. $R_{ON}A$ decreases according to the distance between PBA1s, while the breakdown voltage is almost constant, which indicates that the PBA1s shield the electric field enough to suppress the punch-through of the low doped p-epitaxial layer of the channel.

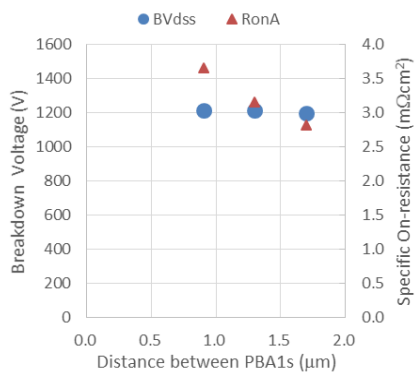


Fig. 4 $R_{ON}A$ and BV_{DSS} depending on the distance between PBA1s of IETMOSFETs with the cell pitch of 10.6 µm.

Figure 5 shows the experimentally measured $R_{ON}A$ and BV_{DSS} depending on the cell pitch from 5.4 µm to 10.6 µm. $R_{ON}A$ linearly decreases according to the cell pitch while maintaining the breakdown voltages, which indicates that the design rules optimized at large cell pitches can be applied at smaller cell pitches. Although the series resistances of the substrate and the back-side contact tend to be estimated smaller on the wafer measurement of small transistors because of the current spreading in the substrate, they are estimated to be less than 0.7 mΩcm^2 from the resistivity of the substrate and the ohmic contact.

Figures 6 show the typical characteristics of conduction and blocking on large transistors of the chip size of 3 × 3mm^2. These characteristics are same as those of small transistors and the threshold voltage is 4.8 V.

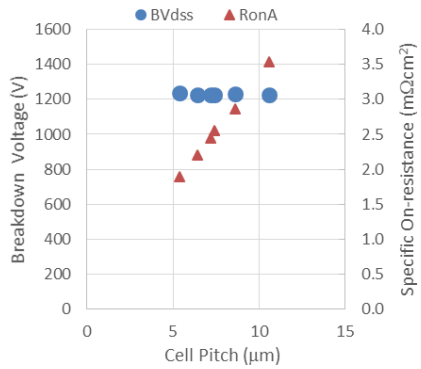
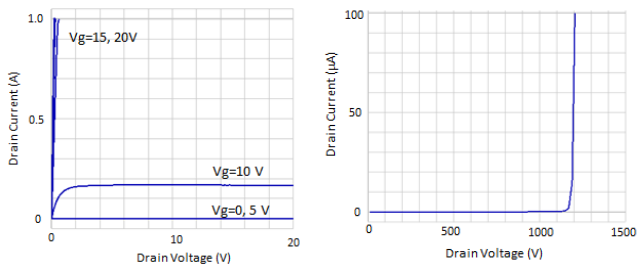


Fig. 5 $R_{ON}A$ and BV_{DSS} depending on the cell pitch from 5.4 µm to 10.6 µm.



(a) (b)

Fig. 6 Characteristics of the transistor of the chip size of 3 × 3mm^2: (a) Conduction and (b) Blocking characteristics.

4. Conclusions

A novel trench SiC-MOSFET named IETMOSFET was proposed and fabricated. PBA1s formed under the bottom of the trench gate effectively reduced the E_{OX} and achieved the high BV_{DSS} above 1200 V. The channels and TCSLs consisted of p- and n-epitaxial layers, respectively, provided the low $R_{ON}A$ of 1.8 mΩcm^2.

Acknowledgements

This work has been implemented under a joint research project of Tsukuba Power Electronics Constellations (TPEC). The authors thank to the members in AIST: Dr. S. Harada for the support of continuing this project, Dr. T. Hatayama (present address: Sumitomo Electric Industries Ltd.) for checking the photomasks and both Dr. Y. Yonezawa and Mr. T. Masuda for fruitful discussions.

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