A Robust 600V GaN HEMT Technology on GaN-on-Si with 400V, 5µsec Load-Short-Circuit Withstand Capability

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Abstract

A 600V normally-ON GaN HEMT technology, featuring an intrinsic Ron×A=500mΩ·mm2 at BVdss~1100V, is described. A novel high-power 30A GaN-Si MOSFET Cascode, with Si-LDMOS back-side source and embedded clamp diode is implemented. For the first time, a 30A-class GaN Cascode is able to withstand 400V, >5µsec load-short-circuit condition, as required in switching inverter applications.

1. Introduction

Wide-bandgap GaN HEMTs have started to be introduced for >100V frequency (MHz) power supplies and ~600V inverter applications [1, 2]. Although compared with Si SJMOSFETs, improvements in efficiency are reported, a lack of short-circuit ruggedness [2, 3] is a hurdle that must be addressed.

In this work, a Normally-ON GaN HEMT, connected in a Cascade configuration with a low-side low-voltage Si MOSFET, is presented. The load-short-circuit withstand robustness was improved by 1) reducing the heat generation and 2) improving device turn-on uniformity in large area arrays.

2. GaN HEMT Technology and Device Description

The GaN HEMTs are fabricated on a dedicated GaN-on-Si 6” wafer in a conventional Si CMOS production line. The GaN epilayer is GaN-cap/AlGaN barrier/GaN channel/GaN Buffer on (111) P-Si substrate. Fig.1 illustrates the GaN HEMT structure. The highly doped p-type silicon substrate acts as back-side Ground Field Plate. A multistep gate electrode and a Source-connected Field Plate (SFP) implemented in Metal-1 (Al) are used to relax the electric field strength at the Drain-side of the Gate/Channel region. The gate leakage current was reduced to 15nA/mm by a SiN gate dielectric. The SiN layers were optimized to stabilize the donor-like traps at the Si/N/AlGaN interface [4] for controlling collapse and long-term Ron characteristics.

Fig.2 shows the ON-state and OFF-state current characteristics of a 30A HEMT. The maximum saturated current is Idmax =0.31A/mm at Vg=0V, Vd=10V, and the intrinsic specific ON resistance is Ron×A= 500mΩ·mm2, realized by a 2-level AlCu metallization and bonding above the active area of the transistor. The leakage currents Id and Ig ≅ 15nA/mm at 650V, and breakdown voltage BVdss ≅ 1100V are demonstrated. Fig.3 illustrates the dynamic Ron of the GaN HEMT. Less than 20% Ron increase in the Vd=0~600V range is achieved.

3. High Power GaN Cascode

To obtain Normally-OFF operation, the Cascode arrangement shown in Fig.4 is adopted. The low-side Si MOSFET integrates a clamping diode with BVz~23V to limit the reverse Gate-Source voltage applied to the GaN device. To reduce the packaging area, and the Source pin parasitic inductance of the SiMOSFET, a novel Si LDMOS with back-side Source was developed. The threshold voltage is Vth=3.5V which is compatible with Si power transistor. The Cascode total ON resistance is Ron=45mΩ.

Short-Circuit Capability Improvement:

During the Short-Circuit event, the GaN transistor operates at full Vd=Vdd (400V) and Id=Idmax, and must be able to withstand this stress by a few µseconds [2]. The physical analysis of the transistor, and TCAD simulations show that the excessive heat generation (Self-Heating) raises the GaN channel temperature above 400ºC and may cause irreversible damage of the transistor. Above the critical temperature Tc, destruction proceeds by (1) thermal runaway and/or (2) material limitations like CTE (Coefficient of Thermal Expansion) mismatches inducing cracks.

GaN devices, due to their very small area (as compared to Si for a given Ron), result in higher transient thermal impedance Zth (∝ 1/Area), further degraded by the multilayer GaN epilayer, which results in reduction of the vertical effective thermal conductivity k_eff [5]. For a large area device, the heat flow is approximately one dimensional and dominated by diffusion for t<50µs. The short-circuit pulse time to reach Tc is for irreversible damage is

\[ t_p = \left[ \frac{k_{\text{eff}}}{D_\text{eff}} \frac{\Delta T_{\text{crit}}}{P_d} \right]^2, \quad P_d = I_{d\text{max}} V_d, \quad \Delta T_{\text{crit}} = T_c - T_e \]  (1)

where D_eff is the thermal diffusivity and T_e is the case temperature. This relation assumes uniform heat generation which may not be the case in large area arrays, where defects induce current concentration and “hot spots”.

1) Heat generation is directly proportional to I_{d\text{max}} and must be minimized. For the Cascode connection,

\[ I_{d\text{max}} \equiv I_{d\text{max,GaN}} \left[ 1 + G_{n,GaN} (R_{\text{on,Si}} + R_p) \right] \]  (2)

where G_{n,GaN} and I_{d\text{max,GaN}} are the isolated GaN HEMT transconductance and Drain current in saturation regime, respectively.
A further consideration is the uniform turn-on of the whole array. In order to operate uniformly, the GaN HEMT array is composed of multi-blocks surrounded by metal-strapped gate interconnect lines, and each block’s gate resistance is equalized from the Gate PAD.

Fig.5 illustrates the measured single-pulse short-circuit test waveform for $V_d=$400V pulse, of a 30A GaN+Si-LDMOSFET Cascode, encapsulated in a TO247 package. The drain current $I_d$ decreases due to self-heating effect. The time to destruction ($t_p$) of this device is 7µs. The TCAD simulated temperature at the hottest point in the channel of the GaN indicates $T_{crit} \approx 430^\circ$C. The dependence of $t_p$ and the normalized pulse power $\left( \frac{P_p}{A} \right)$ (Fig.6) shows agreement with the heat diffusion model proposed by (1). These results suggest that, in this technology, the device destruction is, in fact, initiated by a thermal mechanism.

4. Conclusions

A robust 600V novel GaN HEMT + Si-LDMOSFET Cascode was developed. The limitations and mechanism during short-circuit event were investigated and modeled to improve the ruggedness of the device. Load-short-circuit withstand capability of >5µs ($V_d$=400V) is shown for a 30A-class device, demonstrating the applicability of this technology to switching power inverter circuits.

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References