Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp1082-1083

# Ideal Deep-Subthreshold Characteristics in C-Axis Aligned Crystalline Oxide Semiconductor FET

D. Matsubayashi, M. Tsubuku, T. Takeuchi, S. Matsuda, K. Ohshima, T. Tanaka, A. Shimomura, M. Sakakura, Y. Yamamoto, and S. Yamazaki

Semiconductor Energy Laboratory Co., Ltd., 398 Hase, Atsugi-shi, Kanagawa, 243-0036, Japan, E-mail: dm1141@sel.co.jp

**Abstract**

**An off-state current in oxide semiconductors (OS) FETs using c-axis aligned crystalline Indium-Gallium-Zinc Oxide (CAAC-IGZO) as an active layer is lower than the dectection limit (~ 0.1 pA) of usual electric current measuring instruments. We developed the calculation method in which the value of subthreshold leakage under the detection limit can be expected from the transfer characteristics in the OS FETs. By applying the method, it was found that the subthreshold swing converges to the ideal value in the deep-subthreshold region under the detection limit. This enables to know the required amount of the threshold voltage shift to obtain the desired off-state current, depending on low power applications.**

## 1. Introduction

C-axis aligned crystalline Indium-Gallium-Zinc Oxide (CAAC-IGZO) is an oxide semiconductor (OS) which has a c-axis aligned crystal structure. The use of this material as an active layer of a thin film transistor enabled fabrication of displays with high definition and low power consumption [1]. The OS FET has an extremely low off-state current of the 1 yA order (y: yocto = $10^{-24}$) [2], and its applications have been proposed in the field of low-power-consumption LSIs [3-6]. If the cutoff current $I_{cut}$ (drain current $I_d$ at gate voltage $V_g$ = 0 V) of the OS FET is reduced to the 1 yA order, non-volatile memories can be realized. To that end, the subthreshold leakage is needed to be sufficiently reduced by shifting the threshold voltage $V_{th}$ in a positive direction. However, the subthreshold leakage can be lower than the detection limit (~ 0.1 pA) of usual electric current measuring instruments, and is hard to be estimated in general.

We developed the calculation method in which the subthreshold leakage of $I_d$ < 0.1 pA can be expected from the transfer characteristics ($I_d$ > 0.1 pA) of an OS FET. By applying the method, it was found that the subthreshold swing (*SS*) converges to the ideal value in the deep-subthreshold region of $I_d$ < 0.1 pA, though the SS degrades in the region of $I_d$ > 0.1 pA due to the shallow electron trap levels. The value of $I_{cut}$ (< 0.1 pA) was shown to be of the same order obtained from the memory retention. The method enables to easily know the required amount of the $V_{th}$ shift to obtain the desired $I_{cut}$, depending on low power applications.

## 2. Experiment

Figure 1(a) shows that the cross-sectional STEM image of a fabricated OS FET. The FET has a double-gate top-contact structure in which gate electrodes overlap source and drain electrodes. The active layer is CAAC-IGZO film with relative permittivity $\varepsilon_r$ ~ 15. As shown in the cross-sectional TEM image of Fig. 1(b), this film has a characteristic layered structure in a direction perpendicular to the substrate [1], like the single crystalline $InGaZnO_4$ (Fig. 3(c)). The 20 nm active layer was deposited by DC sputtering using a polycrystalline target with an atomic ratio of In:Ga:Zn = 1:1:1 in an $Ar/O_2$ atmosphere at a substrate temperature of 300 °C. The layers above and below the active layer are wide band-gap materials ($\varepsilon_r$ ~ 15) with thicknesses of 5 nm and 40 nm, respectively. Top and bottom gate insulator films are oxides ($\varepsilon_r$ ~ 4.1) with thicknesses of 20 nm and 60 nm, respectively. The channel width (*W*) and length (*L*) of the FET are 0.8 μm and 0.85 μm, respectively. Transfer characteristics were measured at room temperature by use of a semiconductor parameter analyzer.

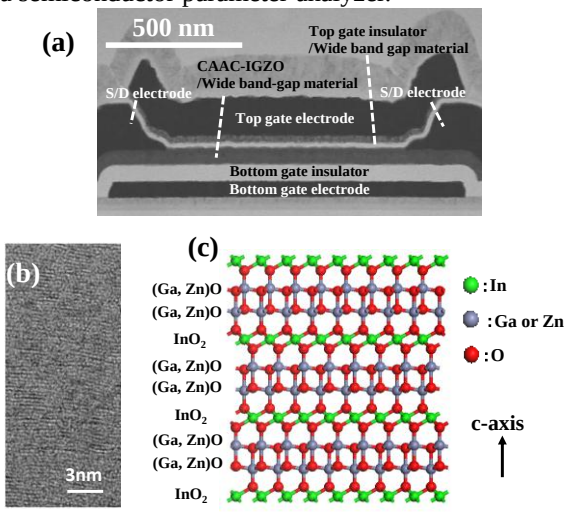


Fig. 1(a) The cross-sectional STEM image of a fabricated OS FET. (b) Cross-sectional TEM image of CAAC-IGZO film. (c) Schematic diagram of $InGaZnO_4$ crystal structure.

## 3. Method

We developed the calculation method in which the interface trap-level density $N_{it}$ is extracted by the comparison between a measured transfer curve and an ideal transfer curve obtained from device simulation. As shown in Fig. 2, when drain current varies from $I_{d1}$ to $I_{d2}$, the gate voltages in measured and ideal transfer curves are assumed to vary by $\Delta V_{ex}$ and $\Delta V_{id}$, respectively, and the surface potential $\varphi_s$ of the active layer is assumed to vary by $\Delta\varphi_s$ in common. In this case, the number (per area and per unit energy) of trapped electrons in the interface levels, $N_{trap}$, can be estimated by the expression,

$$N_{\mathrm{trap}} = \frac{C_{\mathrm{tg}}}{q}\lim_{\Delta\varphi_s\to 0}\left(\frac{\Delta V_{\mathrm{ex}}}{\Delta\varphi_s}-\frac{\Delta V_{\mathrm{id}}}{\Delta\varphi_s}\right)=\frac{C_{\mathrm{tg}}}{q}\left(\frac{\partial V_{\mathrm{ex}}}{\partial\varphi_s}-\frac{\partial V_{\mathrm{id}}}{\partial\varphi_s}\right), \quad (1)$$

where $C_{tg}$ is top-gate capacitance, and $q$ is elementary charge.

The $N_{trap}$ is related to $N_{it}$ by the equation,

$$N_{\mathrm{trap}} = \frac{\partial}{\partial\varphi_s}\int_{-\infty}^{\infty} N_{\mathrm{it}}(E)\,f(E)\,dE, \quad (2)$$

where $f(E)$ is the Fermi distribution function. The $N_{trap}$ obtained from Eq. (1) is fitted by Eq. (2), and then the $N_{it}$は

can be determined. By setting the $N_{it}$ in device simulation, the transfer characteristics including $I_d$ < 0.1 pA can be obtained.

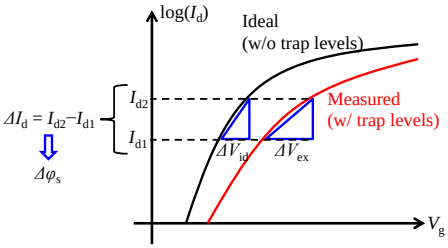


Fig. 2 Schematic diagrams of measured transfer characteristics (with electron trap levels) and ideal transfer characteristics (without electron trap levels).

## 4. Results and Discussion

Figure 3(a) shows the measurement result of the top-gate sweep transfer characteristics of thirteen OS FETs with $W/L$ = 0.8 μm/0.85 μm, under the voltage condition of $V_s$ = $V_{bg}$ = 0 V, and $V_d$ = 0.1/1.8 V. It can be observed that $I_{cut}$ < 0.1 pA is satisfied in all the curves of Fig. 3(a). Figure 3(b) is the extracted $N_{trap}$, by using Eq. (1), from the transfer curve at $V_d$ = 0.1V expressed by the cross marks (×) in Fig. 3(a). The vertical line of Fig. 3(b) is the Fermi energy $E_f$ from the conduction band minimum $E_c$ of the CAAC-IGZO. The $N_{trap}$ seems to have a local maximum just below the $E_c$. From this perspective, when a tail distribution,

$$N_{it} = N_{ta} \exp\left[\frac{E - E_c}{W_{ta}}\right], \qquad (3)$$

was assumed as the $N_{it}$ in Eq. (2), the $N_{trap}$ was well fitted by the dashed line as shown in Fig. 3(b), where fitting parameters were obtained as the peak value $N_{ta}$ = 1.67 × $10^{13}$ $cm^{-2}$/eV, and the characteristic width $W_{ta}$ = 0.105 eV.

The device simulation in which the tail trap levels were set led the transfer curves as shown in Fig. 4. For comparison, the measured points were also plotted. They were well reproduced by the simulated curves. In addition, the subthreshold leakage with $I_d$ < 0.1 pA could be estimated. Though the $SS$ at $I_d$ = 1 pA is 126 mV/dec, the SS at $I_d$ << 0.1 pA converges to 82 mV/dec, which is equal to the ideal value of the OS FET calculated by the expression,

$$SS_{id} = \frac{k_B T}{q}\left(1 + \frac{C_{tg}^{-1} + C_{act}^{-1}}{C_{bg}^{-1}}\right) = 82 \text{ mV/dec}, \qquad (4)$$

where $C_{act}$ is the active-layer capacitance, and $C_{tg}$ and $C_{bg}$ are top-gate and bottom-gate capacitances, respectively, in series between the oxide and the wide band-gap material. The extrapolated value of $I_{cut}$ by using the $SS$ at $I_d$ = 1 pA is estimated to be 1.1 × $10^{-16}$ A. This value is overestimated more than one digit, comparing to $I_{cut}$ = 6.7 × $10^{-18}$ A obtained from Fig. 4(b)

The averaged value of $I_{cut}$ obtained from the transfer curves of Fig. 3(a) for the thirteen FETs was 2.0 × $10^{-18}$ A. On the other hand, the memory in which an OS FET with the same process was connected to a retention node was fabricated. From the memory retention, the $I_{cut}$ was estimated to be of the 1 × $10^{-18}$ A order, which was converted from initial slope of the time dependence in voltage drop of the retention node. Therefore, the $I_{cut}$ = 2.0 × $10^{-18}$ A obtained from Fig. 4(b) is consistent with the value from the memory retention. For example, in order to reduce the subthreshold leakage down to 1 yA, $V_{th}$ needs to be shifted by $SS_{id}$ × [ log($I_{cut}$) − log(1 × $10^{-24}$)] = 0.52 V in a positive direction.

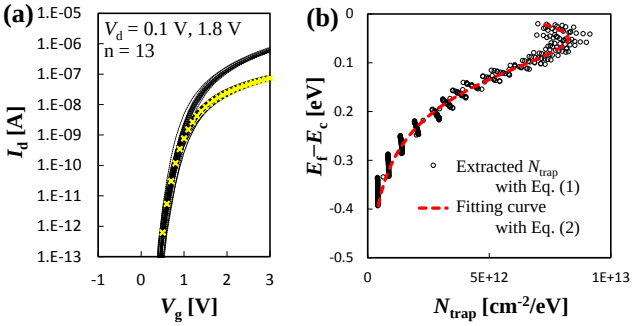


Fig. 3(a) The measurement result of the top-gate sweep transfer characteristics of thirteen OS FETs with $W/L$ = 0.8 μm/0.85 μm, under the voltage condition of $V_s$ = $V_{bg}$ = 0 V, and $V_d$ = 0.1/1.8 V.$W/L$ = 0.8 μm/0.85 μm. (b) The number (per area and per unit energy) of trapped electrons in the interface levels, $N_{trap}$ (○ marks) and the fitting curve (dashed line). The $N_{trap}$ was extracted from the transfer curve at $V_d$ = 0.1V expressed by the cross marks (×) in (a). The vertical line is the Fermi energy $E_f$ from the conduction band minimum $E_c$ of the CAAC-IGZO.

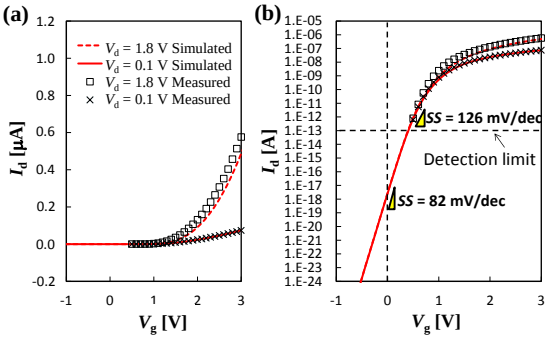


Fig. 4 Comparison between the measured points and the device simulation in which the extracted tail trap levels were set. The vertical axes are (a) linear scale and (b) log scale. While the $SS$ at $I_d$ = 1 pA is 126 mV/dec, the $SS$ at $I_d$ << 1 pA is 82 mV/dec, equal to the ideal value of Eq. (4).

## Conclusion

We developed the calculation method to expect the subthreshold leakage of $I_d$ < 0.1 pA, by extracting interface trap-level density from the measured transfer characteristics of OS FETs. It was shown that the trap-level density is exponentially reduced, as the energy gets away from the $E_c$. This means that the $SS$ to converge to the ideal value in deep-subthreshold region. The method enables to easily know the required amount of the $V_{th}$ shift to obtain the desired $I_{cut}$, depending on low power applications, and to provide benchmark for OS FET process or circuit design.

## References


[1] S. Yamazaki *et al.*, Proc. SID'12 Digest, pp. 183-186, 2012.
[2] K. Kato *et al.*, Jpn. J. Appl. Phys., **51**, 021201, 2012.
[3] H. Inoue *et al.*, IEEE JSSC, **47**, 2258, 2012.
[4] T. Ohmaru *et al.*, Ext. Abstr. SSDM, pp. 1144-1145, 2012.
[5] T. Aoki *et al.*, VLSI Tech. Dig. Tech. Papers, pp. 174-175, 2011.
[6] Y. Kobayashi *et al.*, VLSI Tech. Dig. Tech. Papers, pp. 170-171, 2014.