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Trench Gate Process for 60-nm-Node C-Axis Aligned Crystalline In-Ga-Zn-O Field-Effect Transistors

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Abstract

As an oxide semiconductor field-effect transistor (FET) that achieves both low power consumption and high-speed operation, we fabricated prototype 60-nm-node c-axis aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO) FETs through a simple process using a trench gate, and evaluated their characteristics. The results confirm that a 60-nm-node IGZO FET fabricated through a low-temperature process at 450°C can have a high cutoff frequency up to approximately 20 GHz and show a low off-state current of at most 3×10^{-16} A even at a substrate temperature of 150°C. This study proposes an IGZO FET structure potentially capable of achieving both low power consumption and high-speed operation.

1. Introduction

Oxide semiconductors having a c-axis aligned crystalline (CAAC) or nanocrystalline (nc) structure have recently been researched and developed. Among them, CAAC indium-gallium-zinc oxide (IGZO) has brought a high-resolution, low-power display into reality [1]. Further attempts have been made to apply CAAC-IGZO field-effect transistors (FETs), which are characterized by their extremely low off-state leakage current [2], to memory [3], central processing unit [4], image sensor [5], and other devices. For use in these devices, we are developing FETs capable of operating at a high speed with low power consumption, with the aim of creating distinctive products that are differentiated from existing devices.

Here we propose an IGZO-FET device structure that can be fabricated through a simple process using a trench gate and achieve both low power consumption and high-speed operation, and report the characteristics of IGZO FETs with a 60-nm-node channel length.

2. Experiment

Figure 1 shows an IGZO-FET device structure which we call a trench-gate self-aligned (TGSA) structure.

The TGSA structure in Fig. 1 is formed through a simple process shown in Fig. 2. An IGZO island is formed (element isolation), and an interlayer film is then formed and planarized. Next, a trench is formed by etching the interlayer film and source/drain electrodes, and a gate is formed by gate insulator deposition, gate metal deposition, and chemical mechanical polishing (CMP). By using the trench gate, the gate and the source/drain electrodes are formed in a self-aligned manner. After that, a passivation film, an interlayer film, vias, and wirings are formed. In this manner, we fabricated TGSA IGZO FETs. Treatment such as annealing was conducted as necessary. The TGSA IGZO FETs were fabricated through a low-temperature process at 450°C after the IGZO film deposition.

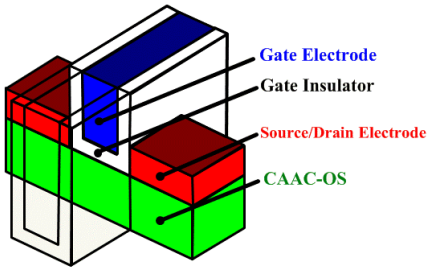

Fig. 1 Bird's eye view of an IGZO-FET structure which we call a trench-gate self-aligned (TGSA) structure.

Then TGSA structure IGZO-FET characteristics measures cutoff frequency (f_T) for high speed operation, and off-state current for low power consumption.

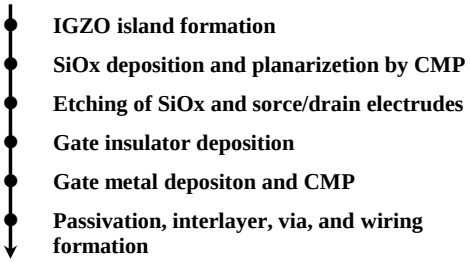

Fig. 2 Process flow for TGSA IGZO FET.

3. Results and Discussion

Figure 3 shows cross-sectional scanning transmission electron microscope (STEM) images of the fabricated 60-nm-node IGZO FET. As shown in Fig. 3, the channel width (W) and the channel length (L) between the source and the drain are each 6X nm.

Figure 4 shows the source-drain current (I_{ds}) and source-gate voltage (V_{gs}) characteristics of our fabricated 60-nm-node IGZO FET. As seen from Fig. 4, the FET has normally-off characteristics; the off-state current at a gate voltage of 0 V was below the detection limit (10^{-13}) of a measurement instrument.

Next, 300 TGSA IGZO FETs were connected in parallel and the relationship between the cutoff frequency and transconductance (g_m) of the FETs was measured. Figure 5 shows the measured cutoff frequency and transconductance of TGSA IGZO FETs that were fabricated through different processes. The measurement was performed at drain-source voltage (V_{ds}) = 2.0 V and V_{gs} = 2.0 V. Figure 5 indicates that the cutoff frequency of the 60-nm-node IGZO FET is close to the approximation of an FET with L = 60 nm; the maximum cutoff frequency is observed to be approximately 20 GHz.

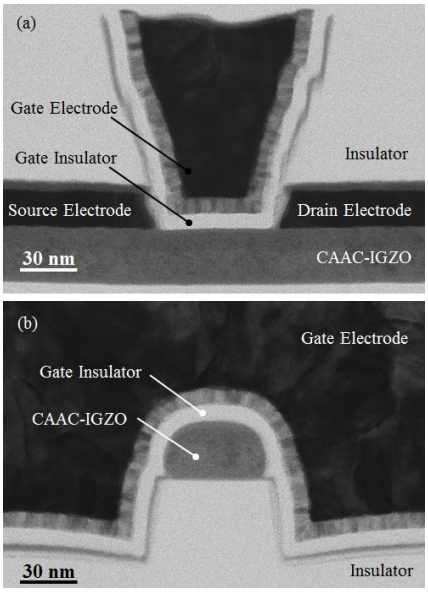

Fig. 3 Cross-sectional STEM images of TGSA IGZO FET: (a) L direction, and (b) W direction.

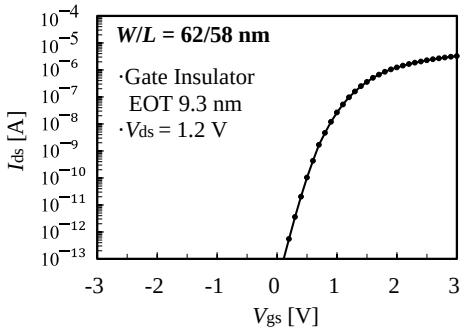

Fig. 4 I_{ds}-V_{gs} characteristics of TGSA IGZO FET.

To measure the off-state current as a function of temperature, a large number of TGSA IGZO FETs were connected in parallel to have a total W of 2.46 μm. Figure 6 shows the I_{ds}-V_{gs} characteristics of the TGSA IGZO FETs as a function of temperature. The current below the detection limit of the measurement instrument was obtained at the substrate temperature ranging from the room temperature (R.T.) to 150°C. It should be noted that the 60-nm-node IGZO FETs each have an off-state current of at most 3×10^{-16} A at 150°C, though Fig. 6 represents a high current value at V_{gs} = 0 V because a large number of FETs are connected in parallel. To sufficiently reduce the off-state leakage current at V_{gs} = 0 V, the threshold voltage should be adjusted so as to further shift in the positive direction.

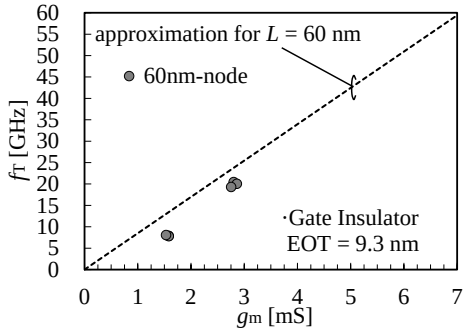

Fig. 5 Cutoff frequency versus transconductance for TGSA IGZO FETs at V_{ds} = 2.0 V and V_{gs} = 2.0 V.

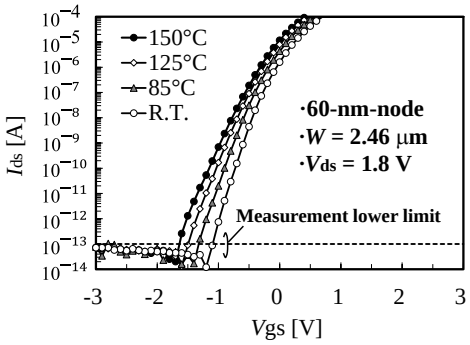

Fig. 6 I_{ds}-V_{gs} characteristics of TGSA IGZO FET at various substrate temperatures.

3. Conclusions

We proposed the TGSA IGZO FET that can be fabricated through a simple process. We produced the 60-nm-node FET and measured the properties. Through a low-temperature process at 450°C, a normally-off FET with W/L = 62/58 nm was obtained. In addition, the 60-nm-node FET was observed to have a maximum cutoff frequency of approximately 20 GHz. Furthermore, the parallel-connected FETs with a total W of 2.46 μm showed the off-state current below the detection limit even at a substrate temperature of 150°C.

We concluded that the TGSA IGZO FET presented significant potential for low power, and high operating speed. We intend to further increase the transconductance, control the threshold voltage, and achieve scaling of the FET.

References

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