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GaAs/$In_{0.2}Ga_{0.8}As$ Fin-Array-Esaki Tunnel Diodes Fabricated on (001) Silicon by Aspect Ratio Trapping

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Abstract

We report the growth of GaAs, $In_{0.2}Ga_{0.8}As$ and GaAs/$In_{0.2}Ga_{0.8}As$/GaAs quantum-well fins of 65 nm width on (001) silicon by the aspect ratio trapping technique. Material properties have been characterized using x-ray diffraction, scanning electron microscopy and transmission electron microscopy. Fabricated Fin-Array-Esaki tunnel diodes exhibit peak-to-valley current ratios of 1.2 at 300 K and 2.6 at 77 K.

1. Introduction

Bottom-up growth of III-V materials on pre-patterned Si substrates by aspect ratio trapping (ART) offers a promising path toward next-generation non-planar transistors [1-3]. Recent advances in nanoscale selective heteroepitaxy in shallow trench isolated Si have led to the demonstration of InGaAs FinFETs [4] and Gate-All-Around nanowire transistors [5] on 300 mm Si substrates. Yet much less effort has been placed on exploiting the ART growth methodology to fabricate heterojunction diodes and HFETs, which is of great interest for ultra-low-power electronics [6]. In this work, we demonstrate GaAs/$In_{0.2}Ga_{0.8}As$ nanowire Esaki tunnel diodes based on fin-arrays grown on V-grooved (001) Si using the ART process. Material properties of the fin structures and device characteristics of the tunnel diodes are presented.

2. Material Growth and Characterization

Metal-organic chemical vapor deposition (MOCVD) was used to grow III-V fins in SiO_2 trenches patterned on exactly orientated (001) Si substrates. The SiO_2 stripes are aligned in the [110] direction, with a height of 160 nm and a pitch size of 130 nm (line: space = 1:1). After surface pretreatment using diluted HF solution, V-grooves were formed by anisotropic KOH etching into the Si substrate. A two-step growth process similar to our previously reported 90 nm-wide GaAs fins [7] has been used. Fig. 1 illustrates the cross-sectional schematic of three fin structures. We first grew the GaAs and InGaAs fins in Fig. 1(a) and (b) in order to obtain the growth parameters for the Esaki diodes in Fig. 1(c). The epilayers of the Esaki tunnel diodes consist of, from bottom to top, a 150 nm Si-doped n-GaAs, a 10 nm Si-doped n-$In_{0.2}Ga_{0.8}As$ and a 100 nm Zn-doped p-GaAs. The carrier densities for the n-type and p-type layers are around $2\times10^{19}/cm^3$. Fig. 2 shows an x-ray reciprocal space map of the (224) reflections measured from the InGaAs fin array in Fig. 1(b). The lattice parameters in the

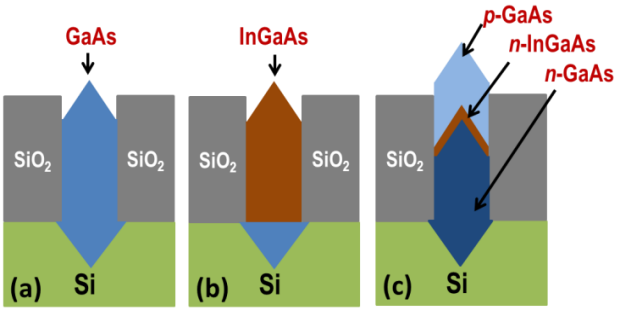

Fig. 1 Cross-sectional illustrations of GaAs, InGaAs and GaAs/InGaAs/GaAs quantum-well fin structures.

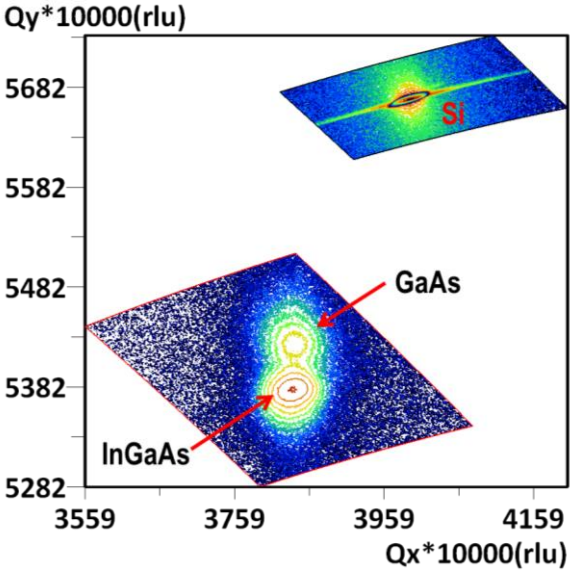

Fig. 2 X-ray reciprocal space maps of the (224) reflections measured from the InGaAs fin array.

growth plane $a_{//}$ and in the growth direction $a_{\perp}$ were determined to be 5.692 Å and 5.767 Å, respectively. The free-standing lattice constant (a_0 = 5.731 Å) and hence the Indium fraction (19.3%) can be calculated from the elastic theory. Both the GaAs buffer in V-grooves and the InGaAs fins were found to be partially strained. Fig. 3(a) and (b) present tilted-view scanning electron microscopy (SEM) image and cross-sectional bright field transmission electron microscopy (TEM) image of the $In_{0.2}Ga_{0.8}As$ fin array, respectively. The growth front of each fin consists of a (001)

surface and two (111)B facets. Most of the stacking faults generated between GaAs and Si are clustered and confined near the hetero-interface. Most of the material in the upper fin region shows good crystalline quality for device applications. A few stacking faults originated from the SiO_2 sidewalls are observed.

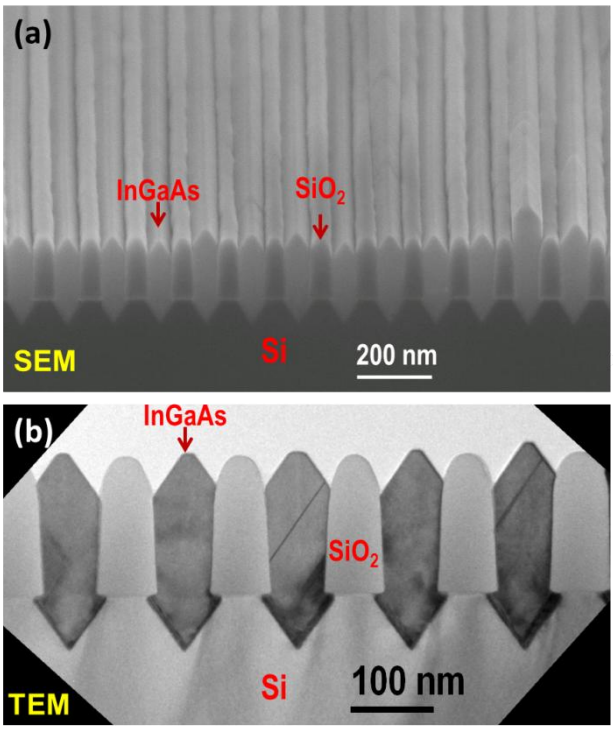

Fig. 3 Tilted-view SEM image (a) and cross-sectional TEM image (b) of the $In_{0.2}Ga_{0.8}As$ fin array.

3. Diode Fabrication and Characteristics

Device fabrication started with formation of the p-metal pad (112 × 60 μm^2) by e-beam evaporation of Ti/Pt/Au and a subsequent lift-off process. Using the p-contacts as a self-aligned mask, the diodes were dipped in H_3PO_4:H_2O_2:H_2O (3:1:50) for 1 min to expose the n-GaAs layer and then soaked in buffered oxide etch for 2 min to completely remove the SiO_2 spacer. N-metal pad (112 × 60 μm^2) was formed by evaporating Ni/Ge/Au metal stack on the exposed n-GaAs fins and lift-off process. Finally, the sample was annealed in N_2 ambient at 300 ˚C for 30s to achieve ohmic contact. The top-view and cross-sectional schematics are shown in Fig. 4(a).

Fig. 4(b) shows semi-logarithmic plots of the current-voltage characteristics of a Fin-Array-Esaki tunnel diode. The observed negative differential resistance at forward bias indicates a well-defined hetero-junction. Peak-to-valley current ratios of 1.2 at 300 K and 2.6 at 77 K have been achieved. Device structure optimization is underway to further increase the current density and peak-to-valley current ratio.

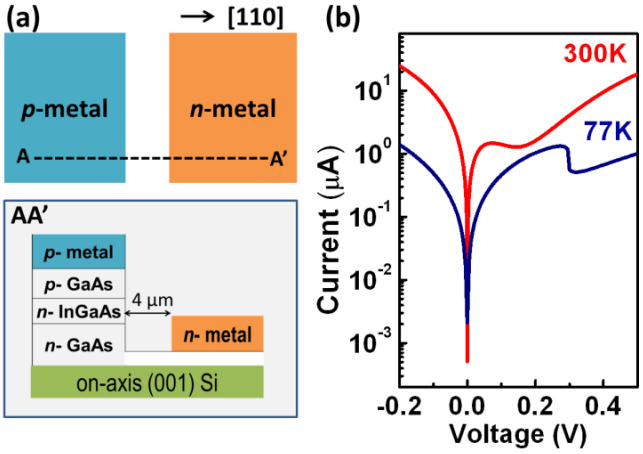

Fig. 4 (a): Top-view and cross-sectional schematics of the diodes; (b): Semi-logarithmic plots of the current-voltage characteristic of a Fin-Array-Esaki tunnel diode.

4. Conclusions

We have applied the aspect ratio trapping technique to grow GaAs, $In_{0.2}Ga_{0.8}As$ fins and GaAs/$In_{0.2}Ga_{0.8}As$ Esaki tunel diodes on (001) Si substrates. The lattice parameters, strain relaxation, growth morphology and defect trapping effect have been characterized. Fin-Array-Esaki tunnel diodes show negative differential resistance and enhanced peak-to-valley current ratio at low temperature as expected in tunnel devices.

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