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Annealing Techniques for Low Temperature Junctions Design in a 3D VLSI Integration

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Abstract

This paper reviews the two main annealing approaches for junctions activation in a 3D VLSI Coolcube™ integration. Optimization guidelines for SPER and laser nanosecond (ns) annealing are given through TCAD simulations and electrical characterizations. Because of the low dopant diffusion in case of both low temperature and ultra-fast thermal annealing the extension first approach for thin film FDSOI devices seems to be mandatory.

1. Introduction

3D VLSI CoolCube™ integration thanks to its stacked devices fabricated sequentially on top of each other enables to achieve very high density and power performance improvement [1]. However, one of the most important challenges is to integrate low temperature devices on the top level without degrading the bottom ones. The reasonable thermal budget to preserve bottom performance has been determined around 550°C for 2 hours [2]. Thus all the transistors technological modules and especially junction activation should be kept below 550°C for a couple of hours. However, reducing the junction anneal temperature below ~1000°C is a major challenge. Two kinds of approaches have been proposed in literature in order to activate the dopant for CoolCube™ devices junctions: the first one is based on the low temperature SPER (Solid Phase Epitaxy Regrowth) [3-5], and the second one, on the use of nanosecond (ns) LTA (Laser Thermal Annealing) [2], [6] which permits to reach very high temperature (1200°C) dopant activation and film recrystallization on a very small time scale and thus without in depth thermal diffusion in the underneath levels.

This paper highlights the interest of these two annealing techniques (Figure 1) and gives optimization guidelines, through TCAD simulations and electrical characterizations of thin film FDSOI integration.

2. Low temperature SPER activation

SPER mechanism is based on the preamorphization of the silicon layer and recrystallization at low temperature (LT) (Figure 2a). Regarding this technique and more generally for LT junction activation, four main challenges have to be faced: first to preserve a crystalline seed during amorphization implant in order to guaranty film recrystallization after anneal, then to avoid or to minimize clusterization phenomenon (inactive cluster leading to carriers mobility degradation), and to avoid dopant deactivation, and finally to place dopants below the spacer in order to connect the channel (Figure 2b). As seen on Figure 3, for n-type doping, the best variant determined on blanket wafer with 22nm of silicon (corresponding to junction last Xlast approach described in Figure 6a), activated @ 600°C 2min is the low dose Phosphorus implant [3]. Regarding p-type doping, the best variant is a co-implant Ge (preamorphization)/B (not seen). However, the lateral diffusion of Phosphorous below the spacer is very low as compared to the usually used HT co-As/P implants (Figure 4) increasing the resistance R_{SP1} under the spacer which contributes mainly to the total access increase [4]. Therefore, an extension first (X^{1st}) integration is proposed (Figure 6a) in FDSOI thin film architectures to reach targeted access resistance (optimized overlap and preservation of a thick enough seed layer [5] (Figures 6b)).

3. Low temperature ns LTA activation

Laser activation is an ultrashort HT annealing technique giving the opportunity to reduce in-depth thermal diffusion (Figure 7a) (for bottom MOSFET performance preservation) while keeping high transistor activation level. First demonstrations have been done with a wavelength of 308nm and pulse duration ~200ns. Laser annealing is very sensitive to geometry and topology. Thus, capping layer over the top transistors was added in order to increase the amount and uniformity of the absorbed laser power (Figure.7b). In addition, to easily modulate the bottom temperature and even to achieve the 550°C on the bottom level, process optimization must be done: the inter-level oxide thickness can be increased, the bottom BOX thickness reduced (down to 20nm), both combined with a shorter pulse duration (100ns) (Figure.8) [2], [7]. Thanks to these optimizations full recrystallization for both NMOS and PMOS planar FDSOI devices has been demonstrated (Figure 9) [2]. As for the SPER case, a sufficient crystalline seed layer thickness should be preserved for limiting the residual defects observed in the NMOS source and drain (Figure 9). The sheet resistance measurements for each dopant species (As, P, BF2) with dose of $1.10^{15}cm^{-2}$ reveals that for a wide range of energy the sheet resistances for laser anneal are of the same order of magnitude as the RTA ones (Figure 9). In addition SIMS profiles confirm the very low doping diffusion (Figure 10) reinforcing the need of X^{1st} junction integration.

4. Conclusions

For CoolCube™ junction activation both SPER and laser annealing face very similar challenges (Figure 12): seed preservation layer and sufficient 2D dopant diffusion below the spacers in order to guaranty high performance top level devices. The most promising solution to encounter these challenges for thin film FDSOI devices is expected to be the X^{1st} integration. The efficiency of these two techniques on others materials like SiGe has still to be evaluated to demonstrate high performance top SiGe PFETs.

Acknowledgements

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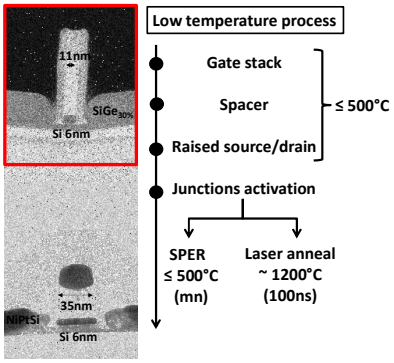


Fig. 1: 3DVLSI TEM Cross-section and Low temperature process steps with different types of annealing technique.

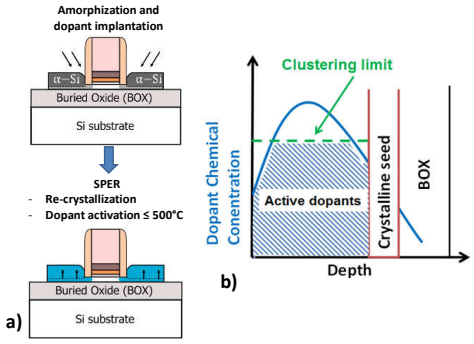


Fig. 2: a) SPER mechanism and **b)** optimization challenges. Seed control; Clusterization phenomenon. Striped areas indicate active dopant regions.

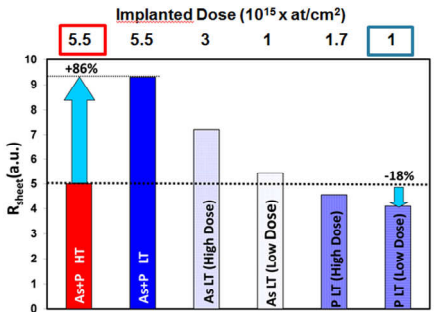


Fig. 3: Rsheet measurements for several dopant types and concentrations on 22nm full-sheet implanted SOI wafers. Best condition for LT: low dose Phosphorus.

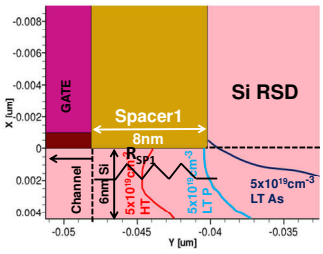


Fig. 4: Evolution of Iso-concentration at $5x10^{19}$at/cm^3 for each dopant of Figure 3.

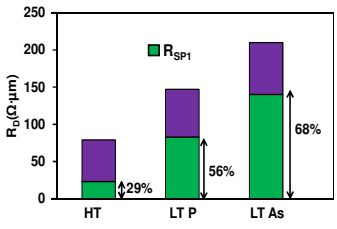
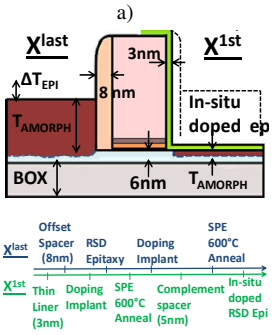


Fig. 5: R_{SP1} contribution extracted by TCAD simulations and percentage of R_{SP1} on total Raccess.



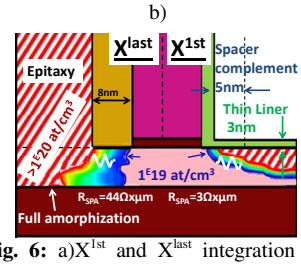
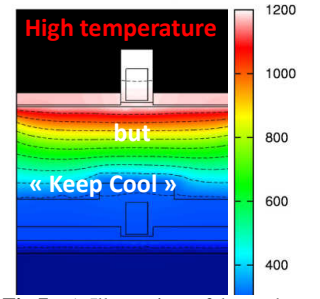
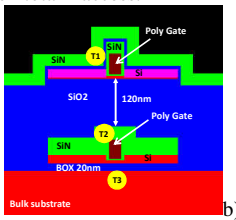


Fig. 6: a)X^{1st} and X^{last} integration description with process flows. b) KMC simulation of junction profile for X^{1st} and X^{last} process flow with SPER.





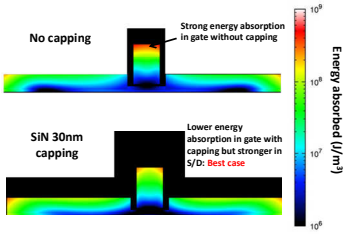
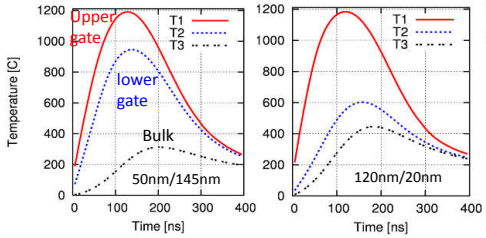


Fig.7: a) Illustration of laser thermal anneal effect on temperature profile b) Optimized 3D simulated structure. SiN 30nm, lower BOX 20nm, inter-level oxide 120nm. Lg 30nm.



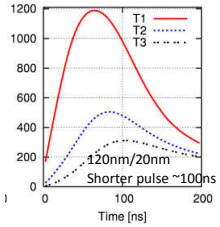


Fig. 8: Temperature versus time for several inter-level oxide and bottom oxide layer. Best case 120nm upper/20nm lower with 308nm wavelength laser and ~200ns pulse duration. T1: T° in the gate stack of the upper layer, T2: T° in the gate stack of the lower layer, T3: T° at top of bulk silicon layer. Very best case with shorter pulse 100ns on the left.

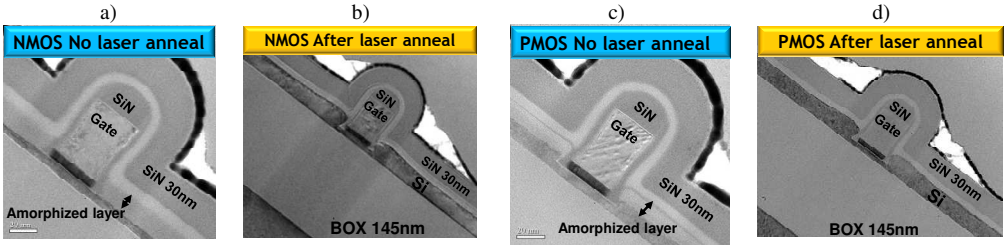


Fig. 9: TEM pictures a) as implanted and b) after laser anneal for NMOS planar FDSOI with As implant. c) as implanted and d) after laser anneal for PMOS with BF2 implant.

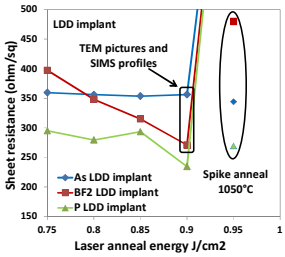


Fig. 10: Sheet resistance measurements for As, BF2, P versus laser anneal energy. RTA spike sheet resistance as reference.

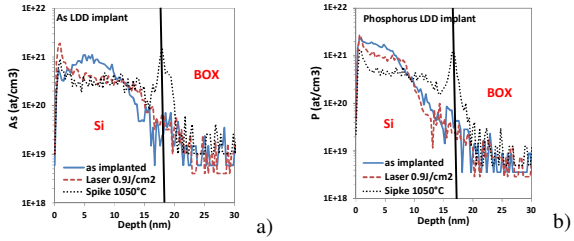


Fig. 11: SIMS profiles for a) As b) P LDD implants: as implanted, after laser anneal at 0.9J/cm^2 and RTA spike 1050°C.

	SPER	LASER (ns)
Tool	Re-use of standard RTP	New tool
Time	some minutes	100ns
Activation	500°C	1200°C
Doping	Need amorphization and implant conditions adaptation	Amorphization (depends on laser wavelength and melt or submelt techniques)
Dopant diffusion	Low	Low
Topology dependence	No	Strong

Fig. 12: SPER and Laser ns anneal comparison

References

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