Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials, Sapporo, 2015, pp1104-1105

# Effects of Microwave Annealing on Ge pMOSFET with Hydrogen-treated Interfacial Layer

Kuei-Shu Chang-Liao[1], Chen-Chien Li[1], Li-Jung Liu[1], Mong-Chi Li[1], Wei-Fong Chi[1], Tzu-Min Lee[1], Tzu-Hsiang Su[1], Chung-Hao Fu[1] and Yao-Jen Lee[2]

[1] Department of Engineering and System Science, National Tsing Hua University
No. 101, Section 2, Kuang-Fu Road, Hsinchu, Taiwan 30013, R.O.C.
Phone: +886-3-5742674, E-mail: lkschang@ess.nthu.edu.tw
[2] National Nano Device Laboratories
No.26, Prosperity Road I, Hsinchu Science Park, Hsinchu, Taiwan 30078, R.O.C.

**Abstract**

**A microwave annealing (MWA) on gate-first Ge pMOSFETs with $H_2$-treated interfacial layer (IL) is studied in this work. The electrical oxide thickness in inversion is scaled down to 0.68 nm; simultaneously, leakage current is about 6.7 x $10^{-4}$ A/cm$^2$. It can be attributed to the enhanced tetragonal $HfO_2$ formation. A low sub-threshold swing and high on/off current ratio in $I_d$-$V_g$ of Ge pMOSFET are obtained thanks to good junction characteristics obtained by a MWA. Due to reduced interface and border traps, a peak hole mobility of 330 cm$^2$/V-s is achieved. The MWA is a promising process for $H_2$-treated IL in Ge pMOSFET.**

## 1. Introduction

Germanium (Ge) has been regarded as a promising channel material in metal oxide semiconductor field effect transistors (MOSFETs) because of its higher carrier mobility as compared to Si [1]. The formation of high-quality Ge oxide formed on Ge is crucial to obtain superior electrical properties of Ge MOSFETs [2]. A $H_2O$ plasma process in an atomic layer deposition (ALD) chamber is proposed to form a high quality interfacial layer (IL) [3, 4]. Although the equivalent oxide thickness (EOT) and leakage current are decreased, the interface trap density ($D_{it}$) needs to be reduced. Hydrogen incorporation is helpful to reduce the $D_{it}$ of Ge MOS devices due to the $H^+$ passivation at $GeO_2$/Ge interface [5]. However, this passivation method needs particular process windows because the unstable $HfO_2/GeO_x$ interface may be degraded by the following thermal treatments. A microwave annealing (MWA) is reported as a useful process for gate-first MOSFETs with high-k/metal gate stacks [6]. The electrical degradation is minimized by a MWA because dopants can be activated with less diffusion and its thermal controllability is better. In this work, impacts of MWA on electrical characteristics of Ge pMOSFETs with $H_2$-treated IL are investigated.

## 2. Experiment

A germanium oxide is grown by $H_2O$ plasma in an ALD chamber. The growth processes include the IL formation and in-situ desorption [4], and then in-situ $H_2$ treatment is carried out for IL passivation in the ALD chamber. Next, a 5 nm HfON dielectric is deposited with in-situ $NH_3$ plasma incorporation in the ALD chamber. Then, a 100 nm TiN metal gate is sputtered and patterned. The source and drain (S/D) are formed by $BF_2$ ion implantation at energy of 30 keV and a dose of 5x$10^{15}$ cm$^{-2}$. Two different thermal treatment is carried out, respectively. One is a sintering at 400 $^o$C for 30 min in a forming gas, and the other is a MWA at 390 $^o$C for 200 s in $N_2$ ambient. The cross-sectional view and detailed process flow of Ge pMOSFETs are shown in Fig. 1.

## 3. Results and Discussion

The X-ray diffraction (XRD) spectra in Fig. 2 (a) shows that the percentage of tetragonal $HfO_2$ (t-$HfO_2$) is increased by a MWA. The cross-sectional transmission electron microscope (TEM) image in Fig. 2 (b) shows that the thickness of high-k dielectric is about 5 nm, and that of IL is about 0.3 ~ 0.4 nm. The inversion capacitance versus gate voltage ($C_{inv}$-$V_g$) in Fig. 2 (c) shows that the electrical oxide thickness in inversion ($T_{inv}$) is scaled down to 0.68 nm. The reduced $T_{inv}$ can be attributed to the enhanced t-$HfO_2$ formation [3]. The dielectric constant (k-value) of HfON with more tetragonal phase is estimated to be about 33. In addition, the leakage current ($J_g$) of the Ge pMOSFET with a MWA is about 6.7x$10^{-4}$ A/cm$^2$ (not shown).

The drain current versus gate voltage ($I_d$-$V_g$) characteristics in Fig. 3 (a) shows that the sub-threshold swing (S.S.) is much reduced (160 mV/dec) and on/off current ratio is enhanced to ~$10^4$ for Ge pMOSFET with a MWA. Fig. 3 (b) shows that the S/D junction leakage can be much decreased by a MWA, which may be due to the reduced defects in S/D junction [7].

Fig. 4 (a) shows that the $D_{it}$ value of Ge pMOSFET with a MWA is lower (~$10^{12}$ /cm$^2$eV) than that with a sintering. Fig. 4 (b) shows that the $N_{bt}$ at around 0.7 nm is reduced by in-situ $H_2$ treatment, and that above 1 nm is obviously reduced by a MWA. Interface and border traps can be well passivated by $H_2$ treatment together with a MWA.

Fig. 5 shows that the peak hole mobility of Ge pMOSFET with a MWA is about 330 cm$^2$/V-s, which is ~15% higher than that with a sintering. The increased hole mobility at a low $N_{inv}$ can be attributed to the reduced coulomb scattering by well passivated IL with $H_2$ treatment. Fig. 6 shows that a high mobility of ~330 cm$^2$/V-s for Ge pMOSFET with a low $T_{inv}$ of ~0.68 nm is achieved by a MWA [1, 8, 9].

## 4. Conclusions

A microwave annealing on gate-first Ge pMOSFETs with $H_2$-treated IL is studied in this work. The $T_{inv}$ is decreased to 0.68 nm, and the $J_g$ is decreased to 6.7 x $10^{-4}$ A/cm$^2$. A low S.S. and high on/off current ratio in Ge pMOSFET are obtained by a MWA due to the reduced leakage current of S/D junction. Both $D_{it}$ and $N_{bt}$ values of Ge pMOSFET are decreased by $H_2$ treatment together with a MWA, and a peak hole mobility of 330 cm$^2$/V-s is achieved as well. Therefore, MWA is a promising process for $H_2$-treated IL in Ge pMOSFET.

## References


[1] R. Zhang *et al.*, *2011 IEEE International Electron Devices Meeting* (2011) 28.23.21-28.23.24.

[2] F. Ji *et al.*, IEEE Electron Device Lett. 32 (2011) 122-124.

[3] C. H. Fu *et al.*, IEEE Trans. Electron Devices 61 (2014) 2662-2667.

[4] C. C. Li *et al.*, IEEE Electron Device Lett. 35 (2014) 509-511.

[5] H. Matsubara *et al.*, Appl. Phys. Lett. 93 (2008) 032104.

[6] Y. J. Lee *et al.*, IEEE Electron Device Lett. 34 (2013) 1286-1288.

[7] T. Yamaguchi *et al.*, *2014 International Workshop on Junction Technology* (2014) 1-4.

[8] R. Zhang *et al.*, *2012 Symposium on VLSI Technology* (2012) 161-162.

[9] C. H. Lee *et al.*, *2013 Symposium on VLSI Technology* (2013) T28-T29.


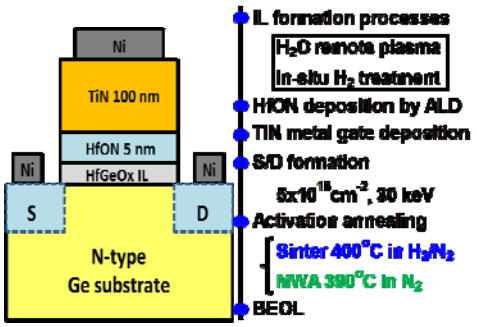


Fig. 1 Cross-sectional view and schematic gate-first process flow of Ge pMOSFETs in this work.

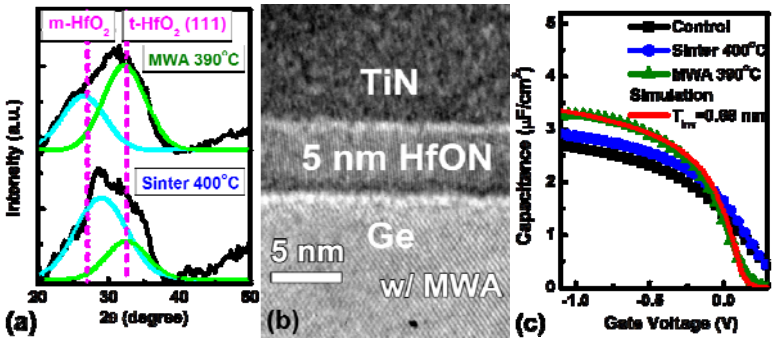


Fig. 2 (a) GIXRD spectra of the samples with a sintering and MWA. (b) Cross-sectional TEM image of sample with a MWA and (c) C-V curves for Ge pMOSFETs in this work.

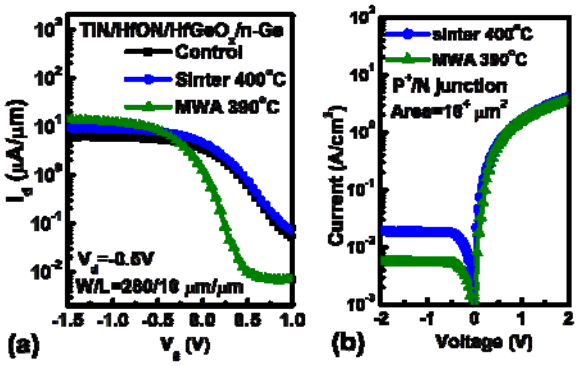


Fig. 3 (a) $I_d$-$V_g$ characteristics of Ge pMOSFETs, and (b) $P^+$/N junction characteristics with a sintering and MWA.

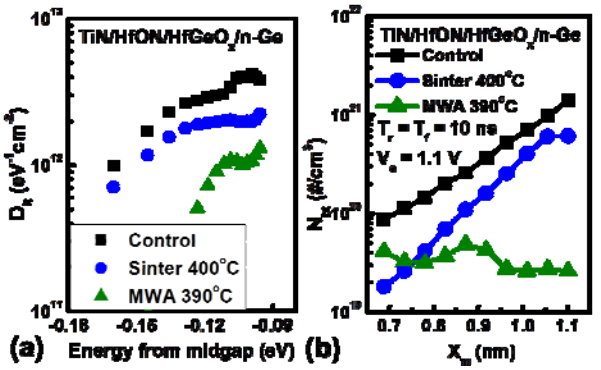


Fig. 4 (a) $D_{it}$ and (b) $N_{bt}$ at different gate dielectric depths for Ge pMOSFETs in this work.

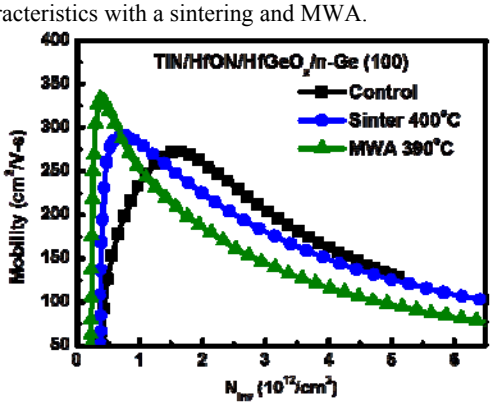


Fig. 5 Hole mobility versus $N_{inv}$ for Ge pMOSFETs in this work.

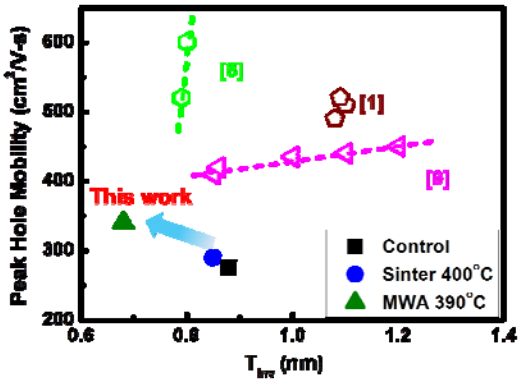


Fig. 6 Peak hole mobility versus $T_{inv}$ for Ge pMOSFETs with different process conditions and some benchmarks.