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Optimization of Extension Doping Condition of FinFETs for Ultra-Low-Power Applications

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Abstract

Influence of extension doping condition on gate induced drain leakage (GIDL) has been investigated to optimize FinFETs for ultra-low-power (ULP) application. Increased GIDL for smaller fin thickness and dependence on the implanted ion species, *i.e.*, larger GIDL for As than for P, are recognized. These results suggest that the residual defects due to extension doping increase the GIDL, and suppression of the defects by optimization of doping is key to realize ULP implementation of the FinFETs.

1. Introduction

Ultra-low-power (ULP) circuits for application of internet of the things (IoT) including smart sensor nodes attract great concern. In a generic MOSFET design, V_t is set so that sufficient on-current is obtained, and the off-leakage is dominantly determined by the steepness of the subthreshold slope (Fig. 1). Introduction of FinFET structure is effective to suppress the subthreshold leakage [1]. In the sub-threshold-voltage (sub-V_t) design to realize ULP [2], V_t is set larger than the supply voltage (V_{dd}) and the off-leakage becomes more sensitive to another leakage mechanism, *i.e.*, gate induced drain leakage (GIDL) as shown in Fig. 1. Therefore, specific process optimization to reduce the GIDL is necessary for the ULP implementation.

In this paper, we focus on suppression of the GIDL of FinFETs for ULP applications. We investigate influence of the fin thickness (T_{fin}) and doping condition of the extension on the GIDL. The guideline for suppressing the GIDL of the FinFETs is discussed based on the measured results.

2. Sample FinFET fabrication

The sample n-type FinFETs are fabricated by a gate first process [3] (Fig. 2). Fin channels with (110)-oriented sidewalls were fabricated from a (100) SOI wafer. T_{fin} was set at 20 or 30 nm for comparison. A TiN metal gate was deposited on a 2.5 nm-thick thermal oxide. After the gate patterning process, ion implantation (I/I) into the fin extension was carried out, in which As or P was selected for comparison. After spacer formation and heavily doping of S/D, rapid thermal annealing (RTA) for the dopant activation was carried out at 870^{o}C, 2 s. Cross section of the fabricated FinFET with T_{fin}=20 nm is shown in Fig. 2.

3. GIDL characterization

I_d-V_g curves at V_d=1 V for the FinFETs with an identical gate length (L_g=100 nm) are shown in Fig. 3. Significant I_d increase is recognized at V_g<0 V due to GIDL. I_d vs gate overdrive (V_{ov}=V_g-V_t) curves are obtained to eliminate the influence of V_t fluctuation (Fig. 4). I_d at V_{ov}=-0.7 V is estimated as the GIDL current (I_{GIDL}). Increasing T_{fin} from 20 to 30 nm, declining tendency of the GIDL is recognized (Figs. 4(a) and (b)). Comparing the extension I/I conditions, the P I/I case (Fig. 4(c)) exhibits declining tendency of the GIDL in comparison to the As I/I case (Fig. 4(b)). The statistical distribution of I_{GIDL} (Fig. 5) reveals these tendency more clearly. Namely, the T_{fin} increase from 20 to 30 nm reduces the median of I_{GIDL} to about 1/10, and the use of P I/I instead of As I/I also reduces it further to about 1/10.

4. Mechanism of GIDL suppression

It is reported that GIDL is enhanced by trap assisted tunneling due to the interface defects [4]. Since the gate stack is identical for all the sample FinFETs (Fig. 2), we focus our attention on the defects caused by the extension I/I. We examine the parasitic resistance, which is affected significantly by T_{fin} [5] and extension doping condition [6,7]. The on-resistance (R_{on}) was measured at linear region (V_d=50 mV) and at sufficient V_{ov} so that it significantly reflects the parasitic resistance, and is compared among different T_{fin} and I/I species (Fig. 6). The case of T_{fin}=20 nm and As I/I exhibits larger R_{on} than the other cases and anomalous scattering of R_{on}. As shown in Fig. 7(a), we consider that damages caused by the extension I/I occupy the whole of the fin for the smaller T_{fin} case, and they cannot be recovered by the subsequent RTA [7]. The residual damage causes the R_{on} increase and its scattering. We consider that the residual damage also increases the GIDL due to the trap assisted tunneling. As schematically explained in Fig. 7(a), the T_{fin} increase from 20 to 30 nm contributes to preserve the undamaged crystal in the fin, resulting in the reduction of the residual damage after the RTA. This contributes to reduce the extension resistance and the GIDL.

The P I/I case also reduces R_{on} in comparison to the As I/I case (Fig. 6). This behavior also coincides with the GIDL reduction. Fig. 7(b) shows nuclear stopping power (S_n) of As and P, *i.e.*, density of the energy transferred to the target Si atoms. As exhibits ~2x larger S_n, namely, it generates larger amount of crystal defects in Si than P. We assume that the use of P with smaller S_n contributes to reduce the residual defects in the fin extension after the RTA, and reduces the GIDL. Generally, the GIDL reduction is carried out by optimizing overlap/underlap of the doped region with the gate electrode [8]. The GIDL dependence on T_{fin} and the extension I/I species provides another process option to manage the GIDL of the FinFETs for ULP applications.

4. Summary

The GIDL of the FinFETs exhibits significant dependence on the fin thickness and the ion species for the extension I/I. The results suggest that suppression of the residual damages due to the extension doping is effective to realize the ULP-FinFETs with the suppressed GIDL.

Acknowledgement

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References

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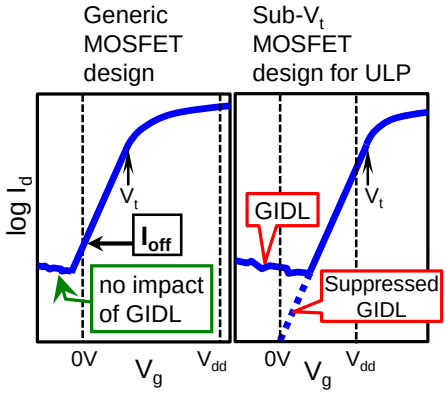

Fig.1 Impact of GIDL on off-leakage (I_{off}) in sub-V_t design. In case of generic MOSFET design, GIDL does not emerge in I_{off}. Care should be taken for GIDL to suppress I_{off} further in the sub-V_t design.

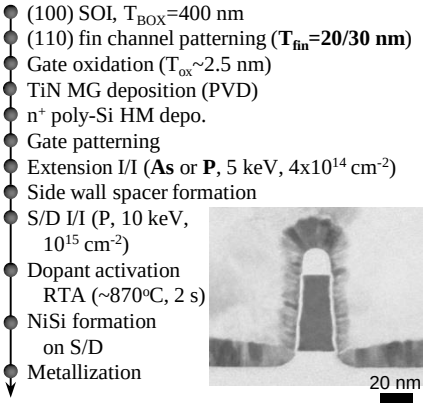

Fig.2 Process flow of sample FinFET fabrication. Fin thickness (T_{fin}) is set at 20/30 nm. Extension doping is carried out by implanting As or P. Cross sectional TEM for the fabricated FinFET with T_{fin}=20 nm is also shown.

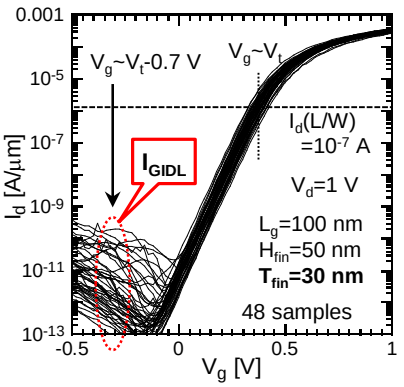

Fig.3 I_d-V_g characteristics of a number of FinFETs with identically designed gate length (L_g=100 nm). We focus on off-leakage at V_g~V_t-0.7 V, at which GIDL current (I_{GIDL}) is significantly recognized.

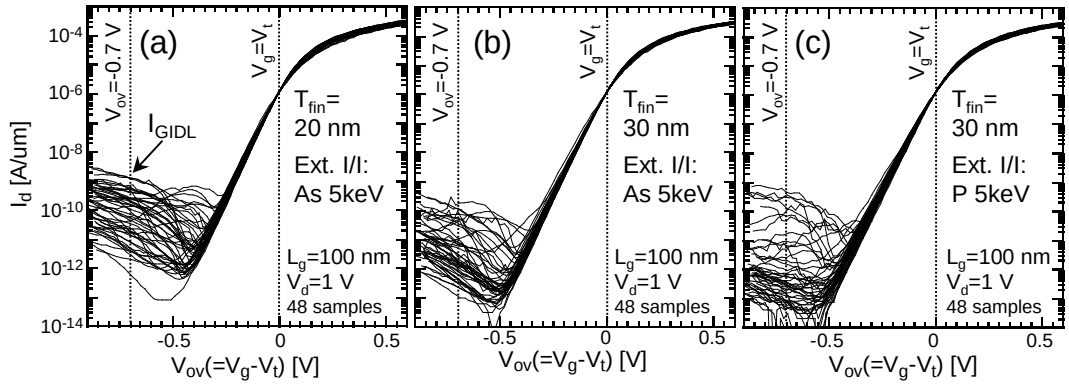

Fig.4 I_d vs gate overdrive (V_{ov}=V_g-V_t) curves for FinFETs with different fin thickness (T_{fin}) and extension doping conditions. The amount of GIDL (I_{GIDL}) is evaluated for identical gate overdrive (V_{ov}=-0.7 V) to eliminate influence of V_t fluctuation. Increase in T_{fin} reduces GIDL, and the P I/I case exhibits smaller GIDL in average than the As I/I case.

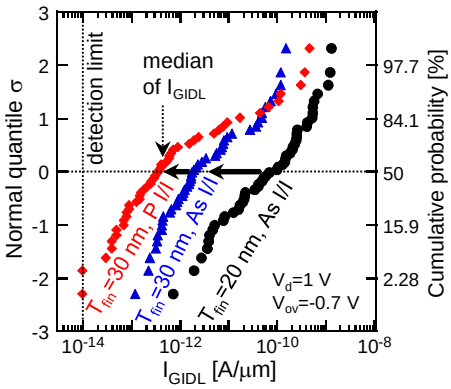

Fig.5 Statistical distribution of I_{GIDL} for FinFETs with different T_{fin} and I/I conditions. Increase in T_{fin} and use of P instead of As improve I_{GIDL} significantly.

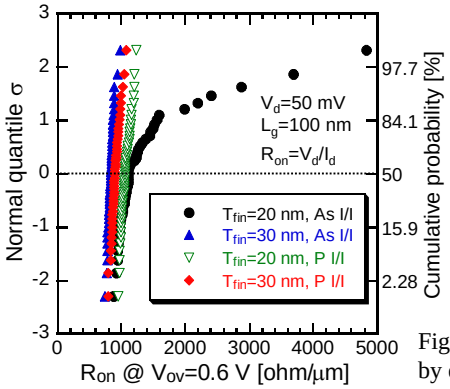

Fig.6 Statistical distribution of on-resistance (R_{on}) for FinFETs with different T_{fin} and I/I conditions. Anomalous increase in parasitic resistance can be suppressed by increasing T_{fin} and use of P instead of As.

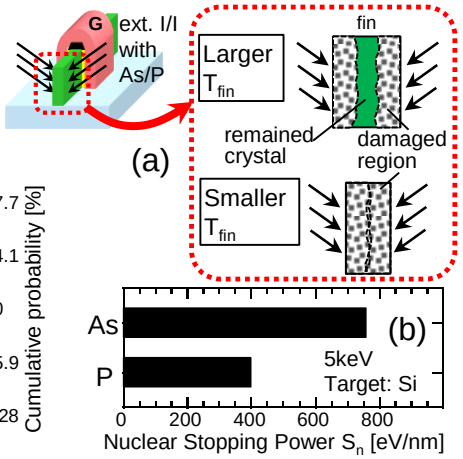

Fig.7 (a) Impact of T_{fin} on damages caused by extension I/I. In case of smaller T_{fin}, fin extension is totally damaged, resulting in unrecovered defects after the activation RTA. (b) Nuclear stopping power (S_n) for As and P with energy of 5 keV. Energy transferred to target Si atoms is ~2x larger for As case, resulting in larger amount of defect formation.