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Ω-Gate Nanowire Transistors Realized by Sidewall Image Transfer Patterning: 35nm channel pitch and opportunities for stacked-Nanowires architectures

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Abstract
Fabrication and characterization of densely integrated Ω-gate nanowire (NW) transistors are presented. An optimized Sidewall Image Transfer (SIT) process has been developed for the patterning of Si NWs and stacked Si NWs with a channel pitch reduced down to 35nm. First demonstration of 60nm high (Si/SiGe/Si/SiGe/Si) multilayer fins associated with a 40nm lateral pitch open the way for stacked-NWs in advanced MOSFET integration.

1. Introduction

Sidewall Image Transfer (SIT) technique overcome standard DUV lithography limits and enables the patterning of features with an actual pitch two times smaller than the one provided by a DUV mask [1]. This technique has already been used to demonstrate SOI FinFETs with a 40 nm pitch [2]. In this work, a new SIT integration scheme is proposed to achieve dense Ω-Gate NW transistors with a 35 nm pitch. This led to the first SIT patterning of 60nm height stacked Si NWs with a 40nm lateral pitch and 17nm width.

2. SIT process and device fabrication

Process is summarized in Fig. 1. A 15nm TiN layer was first deposited followed by a spin-on-carbon (SOC) layer and a Si-rich anti-reflective coating (Si-Arc). A photoresist was then exposed, and developed patterns were trimmed with Cl_2/O_2 before to transfer them into the Si-Arc and SOC layers using respectively CH_2F_2/CF_4/He and HBr/O_2 chemistries. Si-Arc was removed in order to only leave the SOC mandrel. Next step involved conformal deposition of a SiN layer in a process optimized to be highly uniform and controllable. This SiN spacer material was anisotropically etched with $CH_2F_2/O_2/CF_4$ plasma, so that it was completely removed everywhere excepted along the sidewalls of the SOC. A sub-network of hard-mask spacers was left with a spatial frequency of 70nm/2=35nm according to SEM images of Fig. 1. Finally, the SOC mandrels were selectively removed allowing the transfer of the remaining spacers into the TiN and the Si layers using TiN as a masking layer. TEM cross section of two types of devices were realized with either 6 (Fig. 2) or 250 (Fig. 3) parallel Si channels. TEM of Fig. 4 demonstrates aggressive gate length scaled down L_G=16nm. Co-integration with isolated NWs was made possible thanks to a protective SiN hard mask labelled as "no SIT region" in Fig. 1.

3. Electrical results and discussion

Electron (μ_e) and hole (μ_h) effective mobilities in long channel devices are extracted using the split C-V method. In Fig. 5(a) and Fig. 5(b), μ_e and μ_h are displayed *vs* N_{inv} for both 6 and 250 parallel channels. Higher electron mobility is observed in the 250 parallel channels NMOS devices due to a higher T_{Si} as highlighted in Fig. 2 and Fig. 3. A thickness reduction from 8 nm (250 NWs devices) to 5 nm (6 NWs devices) induces an increase of scattering mechanisms (phonon and surface roughness scattering) and thus a μ_e reduction [3]. Alternatively, maximum μ_h is measured at 100 cm^2/Vs for both configurations.

Let's now consider the carrier transport with L_G scaled down to 16nm (Fig. 4). Fig. 6(a) and 6(b) show the I_{ON}-I_{OFF} trade-off for N- and P-FET devices, respectively, for different L_G. For an I_{OFF} current of 100 nA/µm, a drive current I_{ON} of about 650 µA/µm (resp. 290 µA/µm) for N-FET (resp. P-FET) is measured. These are promising values considering the fact that no strain was implemented during the process. As expected, drive current is enhanced with L_G reduction. DIBL benefits from the excellent electrostatic behaviour of NWs geometry according to Fig. 7. Concerning P-FET devices, electrostatic control is less efficient than in NMOS and DIBL reaches 175 mV/V for L_G = 20nm. This can be explained by a stronger diffusion of Boron dopants for PMOS and thus by an effective channel length reduction. This behaviour is confirmed by the subthreshold slope (SS_{SAT}) which stays under 80 mV/dec. (resp. 100 mV/dec.) in NMOS (resp. PMOS) for sub-20nm L_G (Fig. 8). In Fig. 9, typical I_{DS}-V_{GS} curves are shown for two of our devices for L_G=33nm.

Finally, TEM and SEM images of Fig. 10 and Fig. 11 emphasize our perspectives with stacked-NWs. Our SIT process has been successfully validated on $(Si/SiGe)_x$ multilayers leading to the fabrication of either 2 or 3 stacked Si-NWs channels (36nm and 60nm high) with 40nm lateral pitch and an very good regularity.

4. Conclusions

Densely integrated NW-FETs with a 35 nm NW pitch have been fabricated for sub-20 nm L_G. The SIT process has been validated thanks to electrical characterization. Mobility measurements as well as short-channel performances are consistent with previous works and can be further improved using proper technology boosters. Additionally, we present for the first time the patterning of (Si/SiGe/Si/SiGe/Si) multi-layers of 60nm thickness which can be easily used for the stacked-NW transistors making this technology very promising for advanced technology nodes.

References

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[2] T. Yamashita et al., Symposium on VLSI Technology (VLSIT), pp. 14-15, June 2011
[3] Y.-M. Niquet et al., ULIS conference, pp. 49-52, 2012

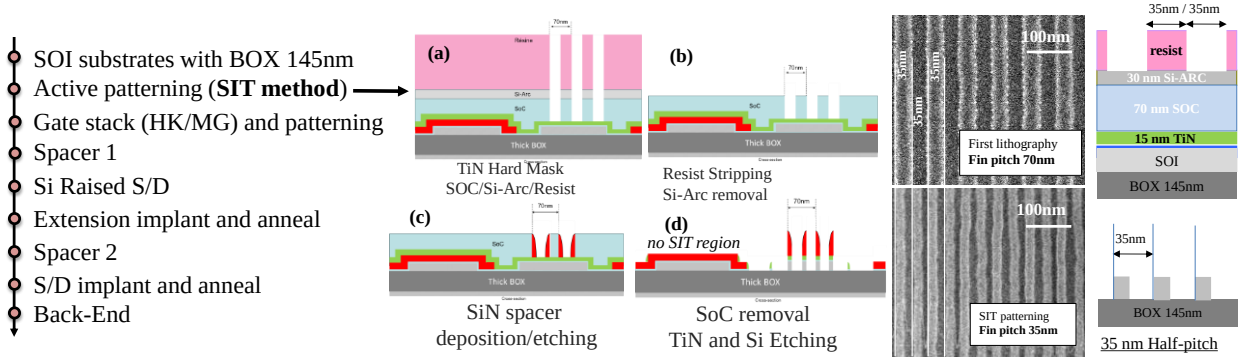

Fig. 1: Process-flow used for the fabrication of dense Ω-gate NW-FETs. The SIT steps are the following: start from 8 nm thick SOI substrate, TiN hard-mask deposition below SOC/Si-Arc/Photoresist (PR) layers for e-beam lithography, SOC opening with Si-Arc removal, SiN spacer deposition and etching, SOC removal, SiN patterns transfer into TiN and SOI, and SiN/TiN removal.

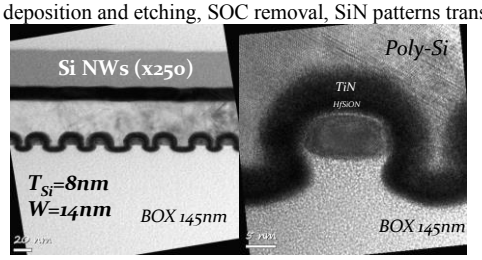

Fig. 2: Cross sectional TEM images of dense omega-shaped-gate nanowire transistors with a NW pitch of 35 nm. NW width and thickness are 14 nm and 8 nm, respectively.

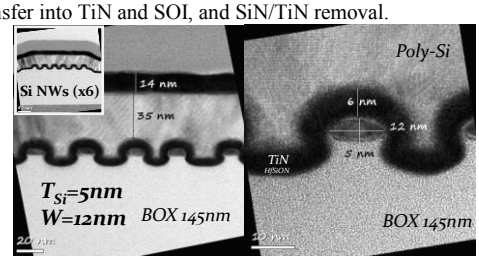

Fig. 3: Cross sectional TEM images of dense omega-shaped-gate nanowire transistors with a NW pitch of 35 nm. NW width and thickness are 12 nm and 5 nm, respectively.

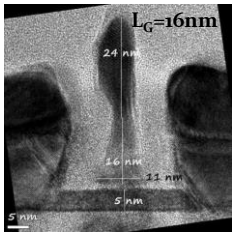

Fig. 4: Cross sectional TEM image of omega-shaped-gate NW transistor with L_G = 16 nm.

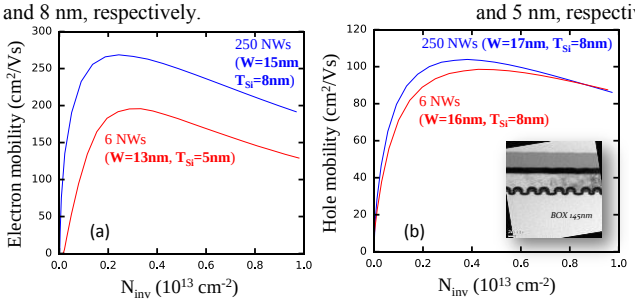

Fig. 5: Electron (a) and Hole (b) effective mobilities of dense omega-shaped-gate nanowire transistors. Basic split-CV method was used on 10 µm gate length devices. Stronger μ_e reduction due to thin T_{Si}.

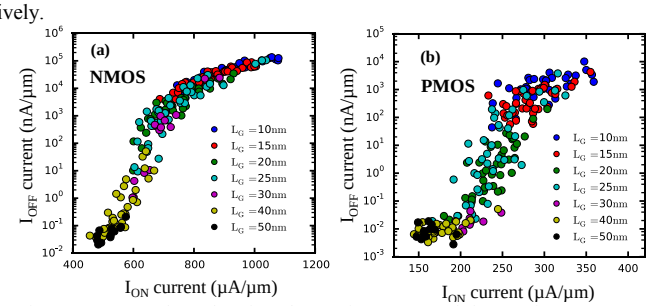

Fig. 6: I_{ON}-I_{OFF} plots showing the performances of dense Si NW (35 nm pitch with 250 channels) transistors for (a) NMOS and (b) PMOS. The drive current is normalized by the effective width defined as W_{eff}= N_{wire}×(2×T_{Si}+W).

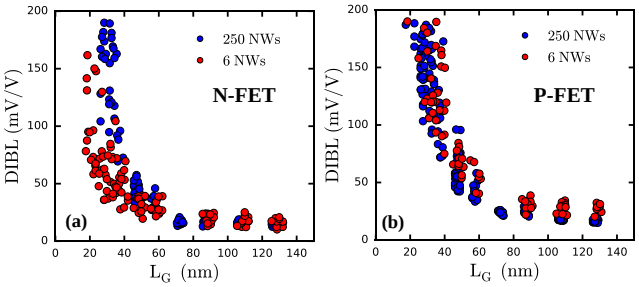

Fig. 7: DIBL as a function of L_G for N-FET (a) and P-FET (b) NW transistors for both 6 and 250 channels devices.

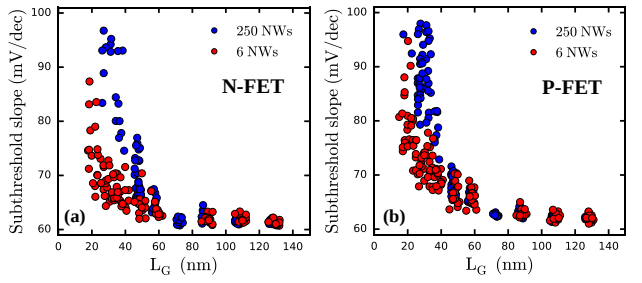

Fig. 8: SS_{SAT} as a function of L_G for N-FET (a) and P-FET (b) NW transistors for both 6 and 250 channels devices.

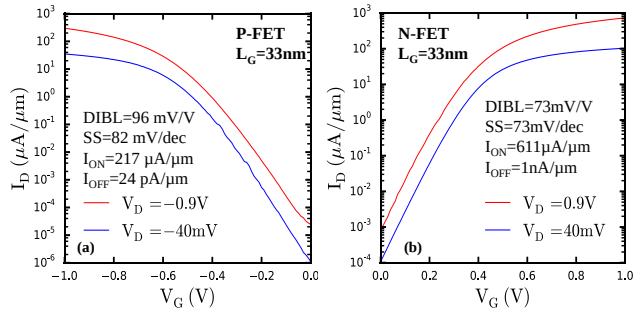

Fig. 9: I_{DS}-V_{GS} electrical characteristics of two of our best scaled devices. (a) P-FET NW transistor with T_{Si}=8 nm, W=14nm and (b) N-FET NW transistor with T_{Si} =8nm, W=12nm.

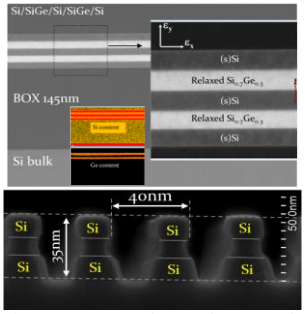

Fig. 10: TEM and SEM images of (Si/SiGe/Si) Fins with a Fin pitch of 40nm and height H=35nm.

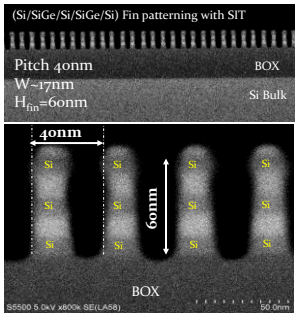

Fig. 11: TEM and SEM images of (Si/SiGe/Si/SiGe/Si) Fins with a Fin pitch of 40nm and height H=60nm.