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A New Method to Induce Local Tensile Strain in SOI Wafers: First Strain Results of the "BOX Creep" Technique

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Abstract

We demonstrate the fabrication of localized tensily strained Si-On-Insulator (sSOI) using a method named BOX creep process. This technique is based on the creep of the Buried OXide (BOX) and consists in the stress transfer from a top sacrificial SiN layer into the thin Silicon layer during a high temperature anneal. Strain and Stress were determined using Raman spectroscopy. Using a compressive SiN on SOI (14 nm Si / 145 nm BOX), we turned relaxed Si into tensile Si with + 1.2 GPa stress.

1. Introduction

Mobility boosters are mandatory to improve the performance of advanced CMOS [1]. Hole mobility is higher for pMOSFETs using compressive Si or SiGe channels whereas electron mobility is higher for nMOSFETs using tensile Si [2]. In the case of Fully-Depleted SOI (FDSOI), tensile sSOI wafers has been developed using Smart Cut™ technology [3]. Unfortunately, they are not suitable for pMOSFETs [2], that is why we explore another approach to fabricate tensile sSOI at a local scale.

2. Experimental details

The BOX creep process (derived from [4]) is summarized in Fig.1. Starting from standard 200 mm SOI wafers, we present recipe conditions so that a 14 nm thick Si on top of a 145 nm BOX can be turned at a local scale into a sSOI structure. The studied process flow is the following:

a) For the first step, a 10 nm thick layer of Silicon oxide is deposited on SOI followed by a compressive silicon nitride (50 or 100 nm). In this study, the SiN is deposited by PECVD (plasma enhanced chemical vapor deposition) and it exhibits a stress of – 2 GPa. The impact of the thickness of this layer (50 and 100 nm) is compared in this study.

b) Then, the MESAs are patterned. Note that for CMOS integration, a basic lithography and etching sequence can be used to apply BOX creep proces for nFET regions only.

c) A high temperature anneal is performed at 1200 °C during 2 minutes under N_2 atmosphere to allow the creep of the BOX layer.

d) The final step consists in the SiN and SiO_2 layers removal using HF and H_3PO_4.

3. Results and discussion

In this study, we focus on 2x2 µm² MESA patterns. We compare two kinds of samples with different SiN thicknesses (50 and 100 nm). We first check that the BOX creep process allows to induce tensile strain in the silicon layer and then confirm that this technique does not create any defects in the final strained Si layer.

i) Strain/stress characterizations

After BOX creep process, the 14 nm thick Si layer has been characterized by Raman spectroscopy in order to estimate the induced stress.

Raman spectra were recorded in the backscattering geometry using a Jobin Yvon T64000 triple monochromator equipped with a liquid N_2 cooled charge coupled device detector. Our measurements were carried out using near-UV excitation wavelength λ at 363 nm with an Ar+ laser. We have used UV-Raman spectroscopy [5,6] to gain access to the stress present in the Si layer. The Raman frequency shift (Δω) extractions allow the calculation of the strain and thus the created stress in the structure (Fig. 2).

The Raman measurement is performed at the center of 2x2 µm² Si MESA. Fig.3 summarizes stress calculations based on Raman shift for strained SOI obtained with 50 and 100 nm Si: The average Δω shifts are -5.7cm^{-1} and -5.4cm^{-1} (for 50 nm and 100 nm thick SiN respectively) which correspond to similar stress levels σ (+ 1.23 GPa and + 1. 20 GPa respectively).

Moreover, scanning Raman extractions shown in Fig.4. for a) 50 nm and b) 100 nm thick SiN confirm the previous results: the stress profiles are identical for both SiN samples. The centers of MESAs present a stress of about + 1.2 GPa (in agreement with Fig. 3) whereas the profiles highlight a slight relaxation at the edges (σ = + 0.9 GPa).

ii) Morphological characterizations

We have also investigated the crystal quality and the top Si roughness of the fabricated sSOI MESAs. The cross sectional STEM micrograph (Fig.5.a-b).) of the Si layer after BOX creep process confirms the good crystallinity of the silicon: no defects are observed in the field.

All the AFM mapping measurements (example in Fig.5.c) confirm the absence of impact of this technique on the Si roughness.

4. Conclusions

We report on the successful fabrication of localized tensily strained Si on Insulator (sSOI) starting from a standard SOI substrate using a new method called BOX creep. The process steps have been detailed and analyzed using advanced characterizations for investigating both the strain (Raman spectroscopy) and the morphological properties of the Silicon layer (STEM, AFM). We demonstrate here local sSOI structures (14 nm Si with + 1.2 GPa stress). Moreover no defects have been observed nor Si roughness degradation.

Acknowledgements

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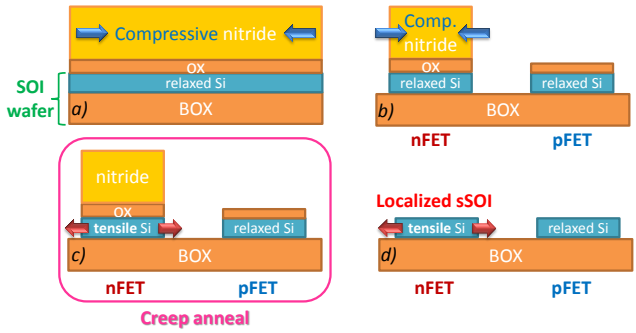

Fig. 1 BOX creep process (starting from SOI wafers) leading to localized sSOI structure for enhanced nFETs: a) SiO_2 and compressive SiN deposition on SOI; b) local SiN etch, MESA patterning; c) creep anneal; d) SiN and SiO_2 layers removal.

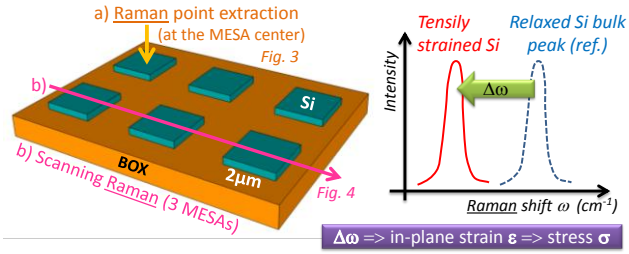

Fig. 2 Schematics of MESA patterns with different Raman measurements and corresponding strain and stress extractions principle.

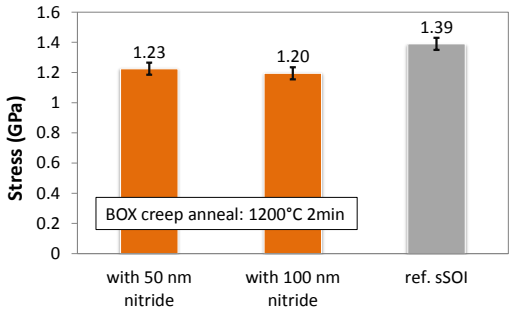

Fig. 3 Average stress calculations from Raman extractions (center of 2x2 µm² MESA) for the 14 nm thick Si film of SOI after BOX creep process with 50 nm and 100 nm thick SiN (+sSOI substrate reference). For each sample, 10 sites have been measured.

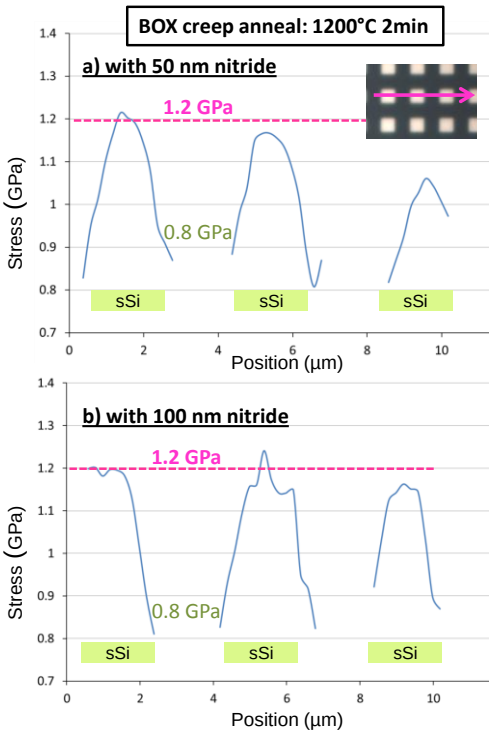

Fig. 4 Stress profiles from 2D Raman extractions for Si MESAs after BOX creep process with a) 50 nm and b) 100 nm thick SiN.

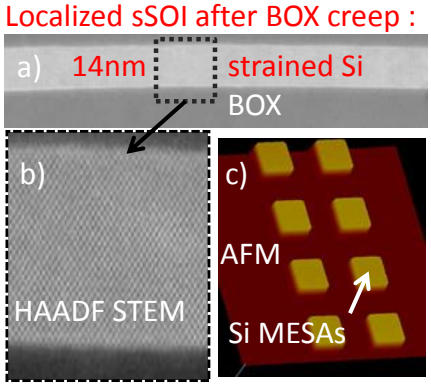

Fig. 5 a-b) Cross-sectional HAADF STEM micrograph of the 14 nm thick Silicon layer after BOX CREEP process. c) AFM mapping of several MESA patterns with no significant roughness.