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High Performance Poly-Ge p- and nMOSFETs Fabricated by Flash Lamp Annealing

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Abstract

High mobility p- and n-type poly-Ge layers were demonstrated employing a flash lamp annealing (FLA) method for monolithically stacked 3D-LSI applications. Tri-gate junction-less (JL) p- and nMOSFETs grown on the layers exhibited high drive current value of up to 311 and 119 μA/μm at a gate-overdrive voltage of 1V, which were comparable with those of a single-crystalline Si-pMOSFET and a poly-Si nMOSFETs, respectively.

1. Introduction

A monolithically stacked 3D-CMOS LSI [1] is attractive to realize higher performance or power efficiency than a conventional TSV- or μ-bump based 3D-LSI because of the higher density of vertical interconnections between the upper and lower CMOS layers. One of key technologies for the 3D-LSIs is a formation process of high-mobility channel layers with low defect densities without introducing thermal damages to the underlying CMOS layers. Although, a layer transfer technique of single-crystal Si layer may be ideal in terms of the channel quality [1], a TFT technology is preferable considering process costs if the TFT performance is comparable with conventional crystalline-Si (c-Si)-MOSFETs. Amorphous-Si, poly-Si and poly-Ge transistors or CMOS circuits on insulator layers have been investigated for that purpose so far [2-4], however, their current drivabilities have been lower than that of c-Si MOSFETs. Therefore, we employed a flash lamp annealing (FLA) method [5] to form high quality poly-Ge MOSFETs to overcome performance of conventional poly- or c-Si MOSFETs. In this paper, we demonstrate (1) high Hall hole/electron mobility of the FLA poly Ge layer, which is larger than drift hole/electron mobility in c-Si, (2) greatly improved current drivability of junctionless (JL) poly-Ge p- and nMOSFETs.

2. Device structure and fabrication

Figure 1 and 2 show schematic of the target device structure of the stacked CMOS devices and the fabrication procedure of the JL poly-Ge p-/nMOSFETs with the FLA process. Since the poly-Ge channels were naturally p-type [5], the channels were undoped for pMOSFETs. Phosphorous (P) ion-implantation (I/I) and activation by the second FLA were used to form nMOSFETs. A flash lamp pulse with a duration of 10ms was irradiated on the amorphous/poly-Ge layer. Gate stack with HfAlO (EOT=1.8nm) gate dielectric/TaN was deposited on the FLA poly-Ge fin channel for p-/nMOSFETs. Self-aligned Ni germanide processes was employed to form source/drain (SD) contact. Inset of the Fig.2 shows schematic structure of the poly-Ge channel tri-gate JL MOSFETs.

3. Results and discussion

The grain size of the n-type FLA poly-Ge layers was found to be typically 3 μm x 300 nm from the electron backscatter diffraction (EBSD) images (Fig. 3). Figure 4 shows lower hole concentration and higher Hall hole mobility for thicker FLA poly-Ge layers before I/I. The Hall hole mobility up to 200 cm^2/Vs was attained for the 100-nm-thick FLA poly-Ge layer. On the contrary, the carrier type was inverted from p- to n-type after the two-step FLA, and the electron carrier concentration saturated to ~$1x10^{19}$ cm^{-3} at the dose levels examined in this work, whereas the electron mobility increased with the dose level up to 140 cm^2/Vs (Fig.5). As shown in the Fig. 6, the obtained Hall hole and electron mobility values overcome the drift mobility of hole and electron in c-Si [6]. Figure 7 shows a cross-sectional TEM image of the n-type poly-Ge fin channel. The fin was considered to be a quasi-single crystalline, since the cross section showed no grain boundary. Figure 8 shows effective hole mobility for the pMOSFET obtained from split C-V measurements. The maximum hole mobility for the poly-Ge pMOSFET was 115 cm^2/Vs, and the value was higher than that of a c-Si/SiO_2 pMOSFET by 22% at the high-electrical field region. Figure 9 shows reasonable I_d-V_g curves of the pMOSFETs and nMOSFETs. The drain current was normalized with fin size; $2xH_{fin}+W_{fin}$. Significant improvement for SD contact formation of up to 10^5 in the type-II devices was observed for nMOSFET, due to the larger offset between the NiGe-edge and the gate-edge. This result indicates that there is a room to optimize cut-off characteristics by adjusting the offset. Figure 10 shows I_d-V_d characteristics of the FLA poly-Ge p- and nMOSFETs. High drain current, I_d of 311(μA/μm) which was comparable to that of c-Si pMOSFET with L_g=60nm node [7] was attained for the pMOSFET and high drain current, I_d of 119 μA/μm was also attained for nMOSFETs.

4. Conclusions

High Hall mobility of up to 200/140 (cm^2/Vs) for p-/n-type poly-Ge layers on insulator layers were obtained by the FLA process. The mobility values were both higher than drift mobility for p-/n-type c-Si with the same carrier concentration. Tri-gate JL p-/nMOSFETs were fabricated on the FLA poly-Ge layers. The high drive current of the pMOSFET exhibited up to 311 μA/μm at V_g-V_{th}=-1V and V_d=-1V which was comparable to that of L_g=60 nm node c-Si pMOSFET, due to the 22% higher effective hole mobility than that of a c-Si/SiO_2 pMOSFET. The nMOSFET also attained high drive current of 119 μA/μm, which was almost the same with the record value [2] of poly-Si nMOSFETs. The high current drivability for p-/nMOSFET indicates that the FLA poly-Ge CMOS will provide great potential for future 3D LSIs.

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References [1] P.Batude et al., IEDM Tech. Dig., 151 (2011). [2] C.C.Yang et al., IEDM Tech. Dig., 731 (2013). [3] Y. Kamimuta et al., VLSI-TSA, 109 (2013). [4] Y. Kamata et al., SSDM2014, F-1-2 (2014). [5] K.Usuda et al., APEX 7, 056501 (2014). [6] C.Jacoboni et al., Solid State Elect. 20 p77 (1977). [7] S. Thompson et al., IEDM Tech. Dig., 61 (2001).

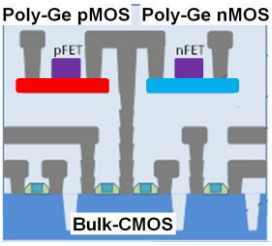

Fig.1 Schematic of monolithic 3D-LSI device formed by sequential stacking of CMOS circuits on underlying CMOS circuits.

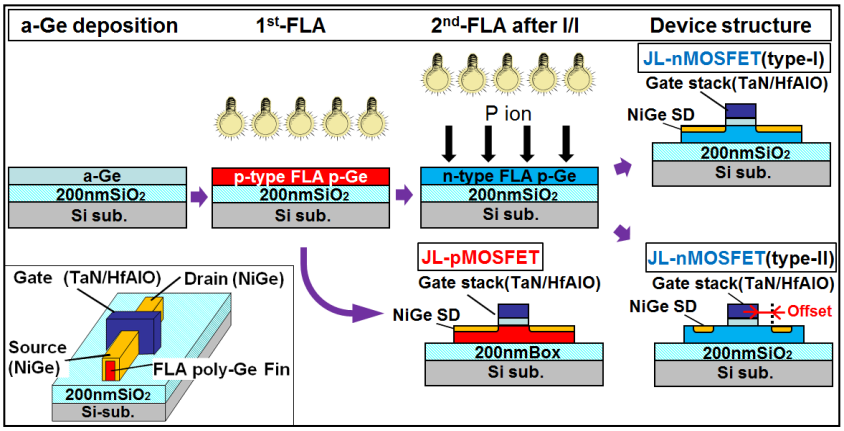

Fig.2 Schematic flow of FLA poly-Ge formation and p and nMOSFET process. Two-step FLA was employed to fabricate junction-less (JL) nMOSFETs. Inset shows schematic structure of the MOSFETs. Two types of SD for nMOSFETs were prepared; Type-I for self-aligned NiGe SD and Type-II for 1.6 μm offse NiGe SD.

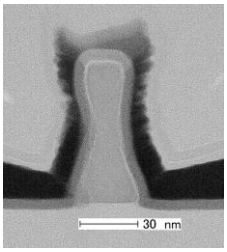

Fig.7 Cross sectional TEM image of a typical n-type two-step FLA poly-Ge fin. Note that the cross section showed no grain boundary.

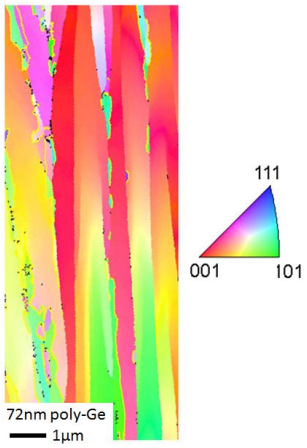

Fig.3 EBSD images of 72-nm-thick P doped ($5x10^{15}$ cm^{-2}) n-type poly-Ge layer grown by the two-step FLA method.

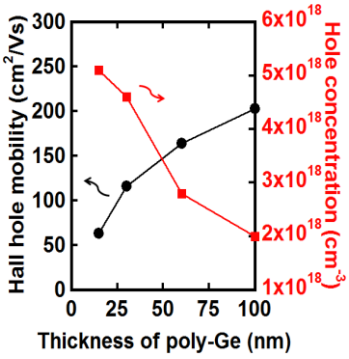

Fig.4 Hole hole mobility and the carrier concentration as a parameter of the FLA poly-Ge thickness.

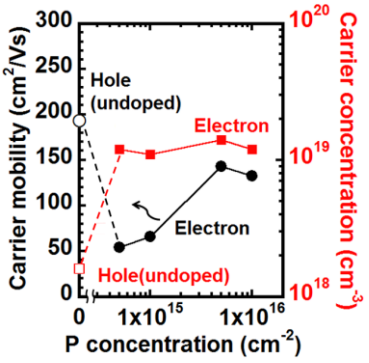

Fig.5 P dose dependence of Hall carrier mobility and the concentration of 72-nm -thick poly-Ge layer grown by two-step FLA method.

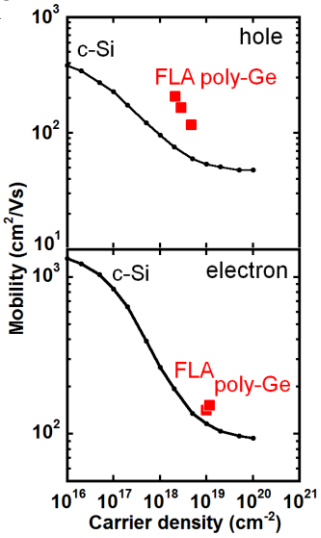

Fig.6 Comparison between Hall hole (upper) and Hall electron (lower) mobility for the FLA poly-Ge (red squares) and reported drift mobility for c-Si.

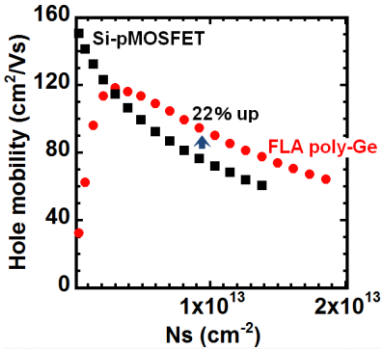

Fig.8 Mobility characteristics for FLA poly-Ge channel tri-gate JL- pMOSFETs obtained by the split C-V method (red circle).

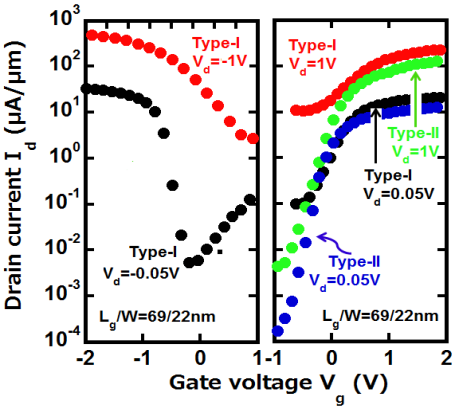

Fig. 9 I_d-V_g characteristics of FLA poly-Ge tri-gate JL pMOSFETs (left) and two-step FLA poly-Ge tri-gate JL nMOSFETs with two types of NiGe SD (Type-I/II) (right). The drain current was normalized by $2xH_{fin}+W_{fin}$.

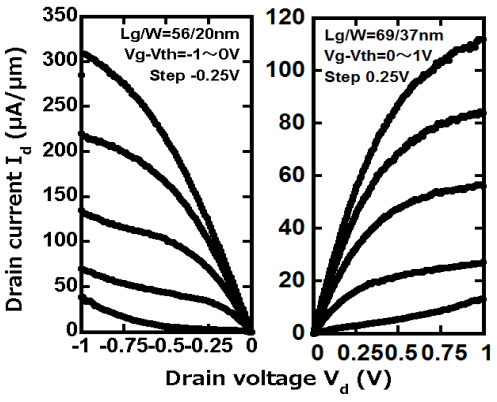

Fig.10 I_d-V_d characteristics of the FLA poly-Ge JL-pMOSFETs (L_g/W_{fin}= 56/ 20nm) (left) and 2-step FLA poly-Ge JL nMOSFETs (L_g/W_{fin}=69/37 nm) (right).