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Thermodynamic Knob for High Performance SiGe Gate Stack Formation

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Abstract

We propose a processing guideline for SiGe gate stack formation based on the oxidation control at SiGe interface. We demonstrate very good C-V characteristics on SiGe with Si-cap free passivation by direct deposition of a dielectric film with optimal post-deposition annealing (PDA). From the results, we conclude the key to the interface passivation for SiGe gate stacks thermodynamically.

1. Introduction

SiGe gate stack formation process is quite different from that of Si or of Ge. In order to lower D_{it}, SiGe interface should be controlled in terms of both dielectric bulk and dielectric/SiGe interface qualities, particularly for Ge-rich SiGe. Thermal oxidation [1], plasma oxidation [2,3] and direct high-k (HK) dielectrics deposition [4] or nitridation [5-7] have been so far tried to achieve a better gate stack on SiGe. An excellent Si-cap free passivation on $Si_{0.5}Ge_{0.5}$ has recently been reported [8]. However, the key to SiGe passivation still remains unclear from materials control viewpoint.

We have surveyed these studies, and have concluded that the following two requirements are essentially critical to control SiGe interface.

(i) How to preferentially oxidize Si of SiGe without GeO_x formation.

(ii) How to suppress Ge pile-up at the interface in the oxidation

The objective of this paper is to propose the thermodynamic guideline for SiGe gate stack formation to meet above requirements, and to demonstrate well-behaved C-V characteristics on Ge-rich SiGe.

2. SiGe oxidation process

In order to meet the requirement (i), we first investigate oxide stability difference between SiO_2 and GeO_2, as shown in **Fig. 1**. The results were calculated by using a thermodynamics database [9]. This calculation result suggests that low oxygen pressure (P_{O2}) oxidation at relatively high temperature seems to be a way to preferentially oxidize Si without GeO_x formation. To confirm this, we oxidized $Si_{0.5}Ge_{0.5}$ in various P_{O2}. The results are shown in **Fig. 2**. By lowering P_{O2}, it is shown that Si is preferentially oxidized, as expected.

To meet the requirement (ii), a thin SiO_2 growth, obtained in low P_{O2}, is needed. An intrinsic challenge, however, is that grown SiO_2 is too thin for gate stacks. Hence, deposited dielectrics rather than oxidation is favored. However, for deposited films, O_2-PDA is generally mandatory to anneal out oxygen vacancies (V_O). This O_2-PDA could eventually deteriorate SiGe gate stacks by oxidized SiGe. To overcome this challenge, we deposit a dielectric film with low O_2 diffusivity and high O_2 affinity (low ΔG^0 in **Fig. 1**), which can keep P_{O2} at SiGe interface very low, and can stabilize bulk dielectric film and hopefully increase k value as well.

Therefore, the question is what dielectric film with low O_2 diffusivity and high O_2 affinity is. On the other hand, taken the lesson from Y-doped GeO_2 [10], we expect that Y incorporation into SiO_2 could also lower O_2 diffusivity of SiO_2 because SiO_2 and GeO_2 share the same crystal structure. Additionally, Y_2O_3 is one of the most stable oxide in terms of the Gibbs free energy and also known to be stable on both Si and Ge, i.e. no metallic reaction between Y_2O_3 and Si or Ge. In this study, we select $YSiO_x$ as a suitable candidate for SiGe passivation.

3. Experimental Details

The starting substrate was 110 nm $Si_{0.5}Ge_{0.5}$(100) on p-Si(100) with resistivity of 5-100 Ω-cm. After SiGe substrate cleaning, $YSiO_x$ was deposited directly on the substrate by rf-co-sputtering of Y_2O_3 and SiO_2, followed by O_2-PDA. Various Y:Si ratios in $YSiO_x$, and O_2 concentrations, temperatures and durations in PDA were investigated. X-ray photoelectron spectroscopy (XPS) with AlKα source was used to study chemical composition of $YSiO_x$ and the IL thickness.

4. Results and Discussion

We first report the O_2 diffusivity of sputtered $YSiO_x$ and SiO_2. **Fig. 3** shows GeO_x thickness grown in PDA of deposited SiO_2 and $YSiO_x$ stacks. The results indicate that no GeO_x forms in $YSiO_x$ stacks while it does in SiO_2 ones, in O_2-PDA at 600ºC. This fact strongly suggests that this process is quite promising for SiGe gate stack formation.

$YSiO_x$/SiGe MOS capacitors (MOSCAPs) were fabricated. **Fig. 4** shows bi-directional C-V characteristics of the Au/$YSiO_x$/SiGe MOSCAPs. From the results in **Fig. 2** and **Fig. 3**, we can expect a slight SiO_2 formation at the interface. If SiO_2 thickness is below 1 nm, the $YSiO_x$/SiGe stack will fulfill the aforementioned requirements (i) and (ii), which is then able to account for the decent C-V characteristics in **Fig. 4**. To confirm this, we measured X-sectional TEM and the IL of SiO_2 was about 1 nm as shown in **Fig. 5**. In addition, the $YSiO_x$/SiGe interface remains very sharp even after PDA at 600ºC.

The dielectric constant of $YSiO_x$ was roughly estimated by changing $YSiO_x$ thickness. **Fig. 6** shows the good linearity in the relationship between EOT and physical thickness of $YSiO_x$, showing that the k value of $YSiO_x$ is about 13. This is higher than expected [10].

Further EOT scalability will be achieved by combining HfO_2-based dielectrics for advanced Si-CMOS.

5. Conclusion

We have proposed and demonstrated the thermodynamics-based engineering knob for SiGe passivation for the first time. Keys are, 1) Ge oxidation should be suppressed, and 2) The IL should be SiO_2 but Si oxidation should be as slight as possible. We have found that deposited films with low O_2 diffusivity such as $YSiO_x$, with optimal O_2-PDA can simultaneously meet those two requirements.

References

[1] F. K. LeGouse *et al.*, *JAP*, **65**, 1724 (1989). [2] P. W. Li *et al.*, *APL*, **63**, 2938 (1993). [3] M. Mukhopadhyay *et al.*, *APL*, **65**, 895 (1994). [4] S. Pal *et al.*, *JAP*, **90**, 4103 (2001). [5] J. Huang *et al.*, *APL*, **88**, 143506 (2006). [6] J. Huang *et al.*, *APL*, **90**, 023502 (2007). [7] J. Han *et al.*, *APE*, **6**, 051302 (2013). [8] P. Hashemi *et al.*, *IEDM* (2014). [9] See www.outotec.com/hsc for HSC CHEMISTRY software 6.1, Outotec Research Oy, Pori, Finland, 2006. [10] C. Lu *et al.*, *APL*, **104**, 092909 (2014).

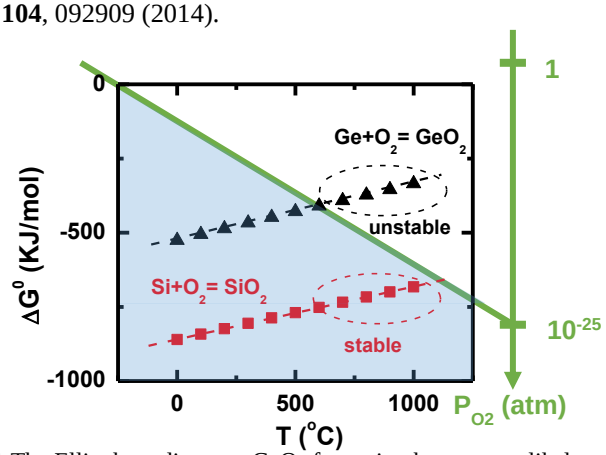


Fig. 1 The Ellingham diagram. GeO_2 formation becomes unlikely as P_{O2} decreases while SiO_2 remains stable. This way offers a pathway to avoid Ge oxidation on SiGe.

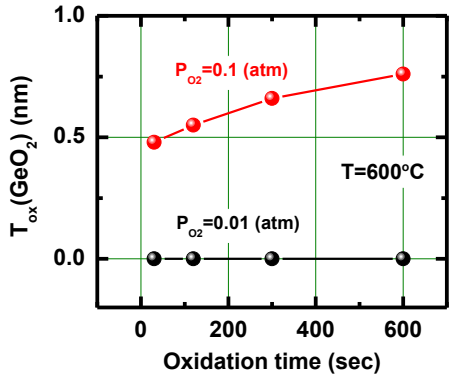


Fig. 2 Ge oxidation rate of SiGe in various P_{O2}. By reducing P_{O2}, Ge oxidation rate is dramatically suppressed. This result confirms the thermodynamic prediction shown in **Fig. 1**.

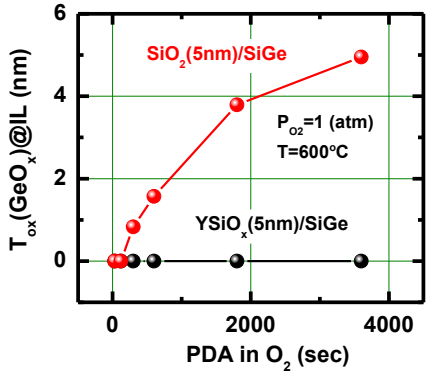


Fig. 3 Ge oxidation rate of SiGe during O_2(1 atm)-PDA in SiO_2 and $YSiO_x$ stacks. The physical thickness of sputtered SiO_2 and $YSiO_x$ were both 5 nm. In case of $YSiO_x$, no Ge oxidation is observed. This is the first observation on SiGe to our knowledge, and is the key results to achieve well-behaved SiGe gate stacks.

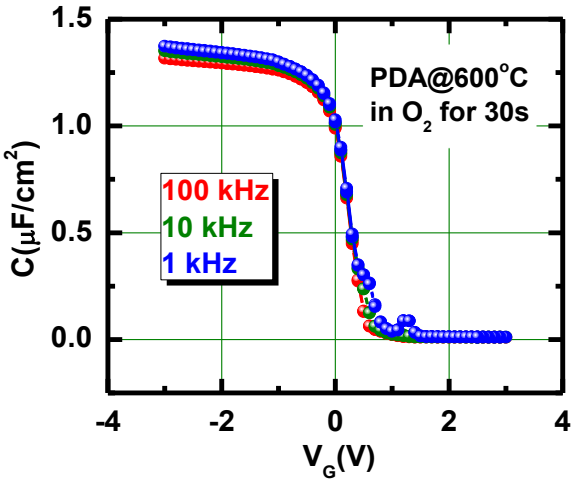
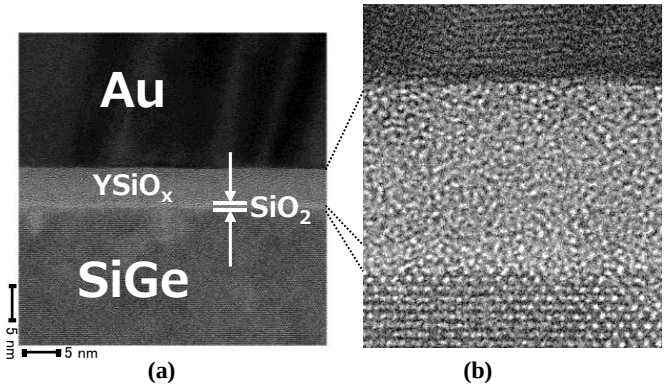


Fig. 4 The C-V curves of an $YSiO_x$(Y:Si=1:1)/SiGe MOSCAP with PDA at 600°C in 1 atm O_2 for 30s. Au and Al are used as top and back contacts, respectively. It was found that PDA at higher temperatures led to larger D_{it}, which might be due to Ge oxidation, while PDA at lower temperatures gave rise to bigger hysteresis possibly due to remaining oxygen vacancy in the bulk (data not shown).



(a) **(b)**

Fig. 5 (a) A TEM image of the $YSiO_x$/SiGe MOSCAP in **Fig. 4**. **(b)** The zoom-in image of the $YSiO_x$/IL(SiO_2)/SiGe interface. This shows the sharp $YSiO_x$/SiGe interfaces of the $YSiO_x$/SiGe MOSCAP even after PDA at 600°C. The thickness of IL of SiO_2 is estimated to be around 1 nm.

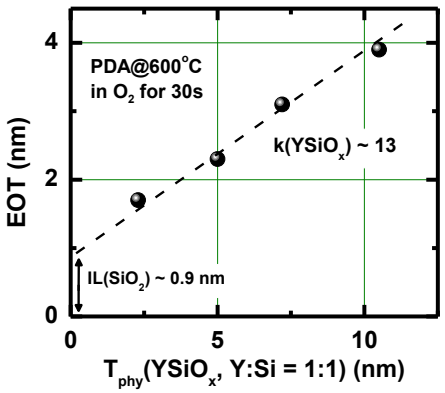


Fig. 6 EOT vs physical thickness to estimate the dielectric constant of $YSiO_x$(Y:Si=1:1) on SiGe MOSCAPs with PDA at 600°C in 1 atm O_2 for 30s. It indicates that k~13, which is higher than as expected, because k of Y_2O_3 is around 12. It might be due to the molar volume shrinking in Clausius-Mossotti relationship. Additionally, the thickness of IL(SiO_2) is extrapolated to be 0.9 nm, which is consistent with the TEM image as shown in **Fig. 5**.