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Engineering high-k/InGaAs interface for extremely scaled gate stacks

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1. Abstract

Ultra-thin InGaAs gate stacks with CET= 0.73 nm (EOT~ 0.6 nm), D_{it} as low as 7.0×10^{11} (cm^{-2} eV^{-1}) and thermal stability up to 600°C is demonstrated by using La_2O_3 as gate dielectric. These results promise the integration compatibility of this gate stack for InGaAs device structures.

2. Introduction

High mobility channel material such as InGaAs is actively being pursued for beyond 10-nm node devices [1]. However, fabrication of high quality dielectric/InGaAs interface with low interface trap density has always been a key challenge. Ideally, high-k material which allow for scaling of the gate stack should be considered as gate dielectric to minimize the effect of high semiconductor capacitance in InGaAs-based devices by improving gate electrostatistics [2]. Table 1 shows a summary of reported high-k dielectric characteristics in three main desired categories for a suitable high-k candidate.

Table 1. Comparison of various high-k on InGaAs

high-k	k-value (scalability)	D_{it} (cm^{-2}/eV)	Temperature tolerance
Al_2O_3[3]	~9 (CET~2nm)	~$8x10^{11}$	~400°C
HfO_2/Al_2O_3[4]	~16/9 (CET=1nm)	>10^{12}	~400°C
HfO_2[5]	~16 (CET~1nm)	>10^{12}	~400°C
ZrO_2[6]	~20 (CET=0.78nm)	>10^{13}	~400°C
La_2O_3	~26 (this work)	this work	this work

Al_2O_3 with a k-value of 9 is commonly used as the gate dielectric in majority of device demonstrations with high performance due to its stable interface with InGaA. As a result, scaling of InGaAs-based gate stacks has been limited due to the lower k-value of Al_2O_3. In this study, we have demonstrated an extremely scalable La_2O_3/InGaAs gate stack with very low interface trap density and higher temperature tolerance compared to Al_2O_3. Furthermore, we report a methodology for fabricating high quality La_2O_3 films by atomic layer deposition (ALD) method.

3. Experimental details

Capacitors were fabricated on S-doped (2×10^{16} cm^{-3}) *n*-$In_{0.53}Ga_{0.47}As$ epiaxially grown on InP substrate. Substrates were first, treated by HF and then dipped in $(NH_4)_2S$ (6%) solution for sulfur passivation prior to La_2O_3 deposition. ALD-La_2O_3 films were grown from precursors lanthanum tris(isopropylcyclopentadienyl) and H_2O at various deposition temperatures. TiN (45nm)/ W (5nm) were in-situ deposited by RF sputtering for gate electrodes. In order to fabricate InGaAs MOSFETs, Ni S/D regions were initially formed on *p*-$In_{0.53}Ga_{0.47}As$ (impurity concentration: 1.8×10^{17} cm^{-3}) and annealed at 250°C. After removal of unreactive Ni, a similar gate stack process flow to capacitors was carried out to complete MOSFETs. Post-metallization anneals (PMA) were carried out in forming gas (F.G.)(N_2:H_2= 97:3%) ambient. CET of the capacitors was extracted by fitting the 100 kHz C-V curve to the ideal curve calculated for InGaAs band structure.

4. Results and discussion

One of the main challenges with depositing high-k material on InGaAs, arises from the fact that in particular surface of InGaAs is rather unstable. As a result low quality surface oxides are easily formed, which degrade interface quality and device's electrical characteristics. Diffusion of elements from the substrate into the gate stack creating additional defects and suboxide species has also been reported [7]. Fig. 1 compares the cross-sectional TEM image of HfO_2/InGaAs and La_2O_3/InGaAs interface after annealing in F.G. at 420°C. Although no visible interfacial layer can be observed for the HfO_2/InGaAs stack, X-ray photoelectron spectroscopy (XPS) data of the same sample reveals the existence of various In, Ga suboxides. This suggests that these elements have diffused from the substrate into the dielectric layer and oxidized within in the dielectric layer.

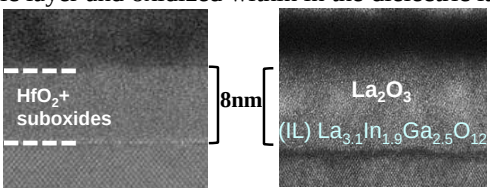

Fig 1. TEM images of 8nm HfO_2/InGaAs and La_2O_3/InGaAs after annealing at 420°C.

On the other hand, TEM image of the La_2O_3/InGaAs sample points to the existence of an interfacial layer. EDX analysis indicate the formation of an amorphous interfacial layer in the form of LaInGaOx. XPS data show that La_2O_3 can react with InGaAs through the formation of Ga-O-La and In-O-La bonds. The composition and thickness of this layer can be manipulated through gate metal selection and PDA process [8].

C-V characteristics of La_2O_3/InGaAs gate stack at 100 kHz with La_2O_3 thickness ranging from 5.5nm to 4.0nm is shown in Fig. 2(a). By optimizing the annealing process and gate stack structure to improve the interfacial layer quality, CET of 0.73nm (including the quantum effect, an

EOT of around 0.6nm) can be achieved. The k-value of ~19 estimated from this thickness series, is much higher than Al_2O_3 and therefore is well scalable. Interface trap density shown in Fig. 2(b), is under 10^{12} ($cm^{-2}eV^{-1}$) even for annealing temperature up to 570°C which is required for gate first processes.

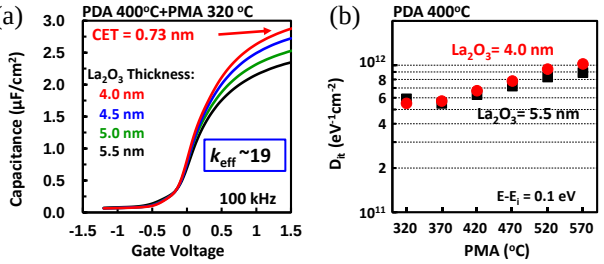

Fig. 2 (a) C-V characteristics and (b) D_{it} of scaled La_2O_3/InGaAs.

In order to synthesize La_2O_3 films by industry standard ALD process which can be used to deposit films on non-planar structures as well as large size substrates, the precursor lanthanum tris- (isopropylcyclopentadienyl) (Fig. 3(a)) was used in these experiments. By using this gas La_2O_3 films can be deposited at relatively low temperatures which suppress the formation of As-oxides and lanthanum hydroxyl groups. The deposition rate of La_2O_3 film extracted from XPS measurements at 150°C, is 0.12 nm/cycle as shown in Fig. 3(b).

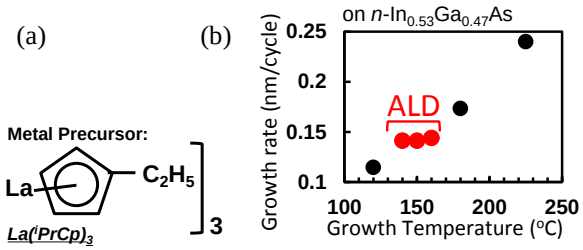

Fig. 3 (a) lanthanum precursor used for ALD-La_2O_3, (b) ALD growth rate dependence on growth temperature.

TEM image of the ALD- La_2O_3/InGaAs interface in Fig. 4, shows a poly-crystalline La_2O_3 with minimum interfacial layer (<0.5nm). Diffraction analysis shows hexagonal crystalline structure for the crystallized parts.

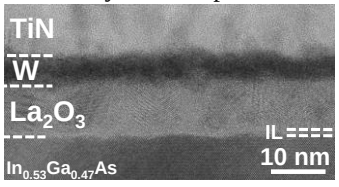

Fig 4. TEM image of ALD-La_2O_3/InGaAs after 320°C annealing.

Excellent C-V characteristics can be measured with ALD- La_2O_3/InGaAs gate stack, shown in Fig. 5(a). Very small frequency dispersion at a frequency range of 5k~1MHz and near ideal 100kHz curve, point to a superior interface quality. The benchmark in Fig. 5(b), shows that even extremely scaled La_2O_3/InGaAs capacitors have smaller D_{it} on the order of 10^{11} (cm^{-2} eV^{-1}) compared to other high-k oxides. However it should be stated that scaling of ALD- La_2O_3 films require a lot more effort.

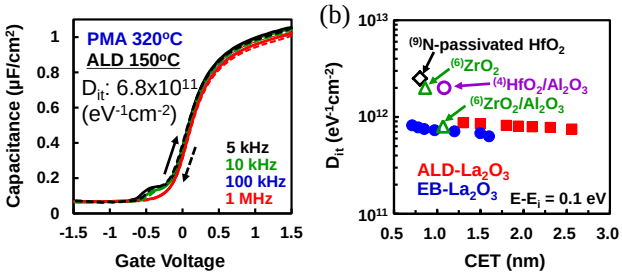

Fig. 5 (a) C-V characteristics of ALD-La_2O_3/InGaAs, (b) benchmark of D_{it} for various scaled high-k

The above results suggest that the concept of forming a high quality reactively formed layer at the interface of dielectric and InGaAs substrate by using La_2O_3 can be applied for InGaAs MOS devices. We also believe substrates with various In contents and orientations can benefit from the same approach. Further investigation is needed to prove that. InGaAs MOSFET operation with ALD-La_2O_3 as gate dielectric and Ni as metal S/D is demonstrated in Figs. 6(a) and (b). Mobility values exceeding that of Si-universal is achieved for a gate stack with CET= 1.1 nm.

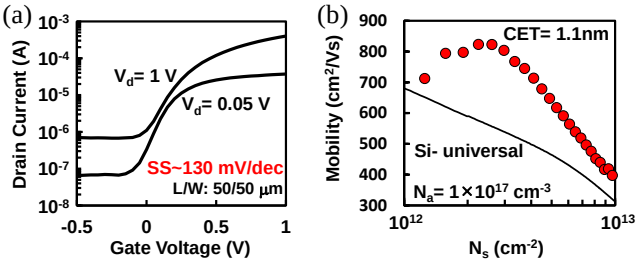

Fig. 6 (a) I_d-V_g and (b) mobility of planar InGaAs MOSFET with ALD-La_2O_3.

5. Summary

We have demonstrated La_2O_3 gate stack characteristics on planar InGaAs and described the fundamentals of La_2O_3 interaction with InGaAs. The scalability, low D_{it}, and thermal stability of La_2O_3/InGaAs combined with a viable ALD solution, indicate that La_2O_3 can be considered for InGaAs-based devices where scaling the gate stack and high thermal integrity are required.

Acknowledgements

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