Impact of La$_2$O$_3$ Interfacial Layers on InGaAs MOS Interface Properties in ALD Al$_2$O$_3$/La$_2$O$_3$/InGaAs Gate Stacks

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Abstract

We examine the electrical and physical properties of ALD La$_2$O$_3$/InGaAs and Al$_2$O$_3$/La$_2$O$_3$/InGaAs MOS interfaces. An InGaAs interface with thick ALD La$_2$O$_3$ provides low interface state density ($D_{it}$) with the minimum value of $3 \times 10^{11}$ cm$^{-2}$eV$^{-1}$, while slow traps in La$_2$O$_3$ cause the large hysteresis. It is found, on the other hand, that Al$_2$O$_3$/0.4nm (10 cycle) La$_2$O$_3$/InGaAs gate stacks can realize $D_{it}$ lower than the conventional Al$_2$O$_3$/InGaAs MOS interfaces, with maintaining small hysteresis.

1. Introduction

High $D_{it}$ at InGaAs MOS interfaces is still a critical issue for MOS-based InGaAs devices. It has recently been reported [1-3] that La$_2$O$_3$ on InGaAs can improve the MOS interface quality and that TiN/Al$_2$O$_3$/InGaAs gate stacks with $D_{it}$ of $8 \times 10^{11}$ cm$^{-2}$eV$^{-1}$ can be realized by using EB-deposited La$_2$O$_3$ and in-situ TiN/W metal gate with an optimized annealing. However, ALD La$_2$O$_3$/InGaAs MOS interface properties have not been fully examined yet. Thus, in this study, we study the electrical and physical properties of ALD La$_2$O$_3$/InGaAs MOS capacitors and systematically examine the effects of inserting thin La$_2$O$_3$ as an interfacial layer on the InGaAs MOS interface properties in the Al$_2$O$_3$/La$_2$O$_3$/InGaAs gate stacks.

2. Experiments

We fabricated MOS capacitors on Si-doped n-In$_{0.53}$Ga$_{0.47}$As ($N_D \sim 5 \times 10^{15}$ cm$^{-2}$) grown on (100) n-InP. After sulfur pre-treatment in a (NH$_3$)$_2$S solution, La$_2$O$_3$ and Al$_2$O$_3$ films were deposited by ALD. La$_2$O$_3$ ALD was performed at the deposition temperature of 150$^\circ$C by using La(PrCp)$_3$ and H$_2$O as the precursors. Also, Al$_2$O$_3$ ALD was performed at 250$^\circ$C by using Al(CH$_3$)$_3$ (TMA) and H$_2$O. Au and Al were deposited by thermal evaporation as the gate metal and the back contact, respectively. Post metallization annealing (PMA) in N$_2$ at 300$^\circ$C for 1 min was performed for all the MOS capacitors.

3. Results and discussions

The C-V curves of the ALD La$_2$O$_3$/InGaAs MOS capacitors with La$_2$O$_3$ thickness of 8.2, 5.2 and 2.9 nm are shown in Fig. 1. The large hysteresis in the 8.2 nm La$_2$O$_3$/InGaAs MOS capacitor is attributed to a large amount of slow traps in the La$_2$O$_3$ films. The decrease in hysteresis with thinning the La$_2$O$_3$ thickness is attributable to the reduction in the surface density of traps in La$_2$O$_3$. The energy distribution of $D_{it}$ estimated by the conductance method for the 2.9 nm La$_2$O$_3$/InGaAs MOS capacitor is shown in Fig. 2 with the reported $D_{it}$ value of TiN/W/La$_2$O$_3$/InGaAs [2]. The present La$_2$O$_3$/InGaAs MOS capacitor is found to have quite low $D_{it}$ of $3 \times 10^{11}$ cm$^{-2}$eV$^{-1}$. These results indicate that ALD La$_2$O$_3$ can provide the excellent passivation effect for InGaAs surfaces with low $D_{it}$, while a large amount of slow traps included in La$_2$O$_3$ can be a critical issue for La$_2$O$_3$/InGaAs interfaces.

Therefore, we have combined ultrathin La$_2$O$_3$ interfacial layers with Al$_2$O$_3$ capping layers in order to simultaneously satisfy small hysteresis and low $D_{it}$ in InGaAs MOS interfaces. Fig. 3 shows the C-V curves of Al$_2$O$_3$/InGaAs gate stacks as a parameter of the La$_2$O$_3$ ALD cycle numbers from 0 to 40 cycles (2.9nm). It is found that the hysteresis is small for the thin La$_2$O$_3$ interfacial layers (10 cycles: 0.4 nm) and becomes larger with an increase in the cycle numbers and the thickness of La$_2$O$_3$. This result confirms us that the hysteresis is attributable to slow traps in La$_2$O$_3$. Fig. 4(a) and (b) show the energy distributions of $D_{it}$ of the Al$_2$O$_3$/La$_2$O$_3$/InGaAs gate stacks as a parameter of the La$_2$O$_3$ ALD cycle numbers and the La$_2$O$_3$ ALD cycle number dependence of $D_{it}$ at the surface energy of 0.1 eV from the midgap (E - $E_F$), respectively. It is found that the insertion of the La$_2$O$_3$ interfacial layer reduces $D_{it}$ and that the increase in the La$_2$O$_3$ thickness decreases $D_{it}$. These results clearly demonstrate the effectiveness of the Al$_2$O$_3$/La$_2$O$_3$/InGaAs gate stacks. On the other hand, the $D_{it}$ values of Al$_2$O$_3$/InGaAs with comparatively-thick (2.9nm) La$_2$O$_3$ are not as low as those of La$_2$O$_3$/InGaAs. On the other hand, Fig. 5(a) and (b) show the energy distributions of $D_{it}$ of the Al$_2$O$_3$/La$_2$O$_3$ (0.4nm)/InGaAs gate stacks as a parameter of the capping Al$_2$O$_3$ thickness and the Al$_2$O$_3$ thickness dependence of $D_{it}$ at 0.1 eV (E - $E_F$), respectively. It is found that $D_{it}$ of Al$_2$O$_3$/La$_2$O$_3$ (0.4nm)/InGaAs gate stacks is reduced with a decrease in the Al$_2$O$_3$ thickness. The findings in Fig. 4 and Fig. 5 suggest some reaction of Al$_2$O$_3$ with the La$_2$O$_3$ interfacial layer, which leads to the $D_{it}$ increase.

We analyzed Au/Al$_2$O$_3$/La$_2$O$_3$/InGaAs gate stacks by TEM and EDX in order to evaluate the physical structure. Fig. 6 shows TEM images of the Au/Al$_2$O$_3$/InGaAs and the Au/Al$_2$O$_3$/La$_2$O$_3$/0.4 nm/InGaAs gate stacks. It is observed for the Au/Al$_2$O$_3$/La$_2$O$_3$/InGaAs gate stacks that there are two insulating layers. In addition, the thickness of the lower layer 1.5nm is much thicker than 0.4 nm, suggesting any interface reaction between La$_2$O$_3$ and Al$_2$O$_3$. To clarify the compositions of the insulators, the depth profile of In, Ga, As, Al and La were analyzed by EDX. Fig. 7 shows the depth profiles of the atomic percentages of In, Ga, As, Al and La of Au/La$_2$O$_3$ (2.9nm)/InGaAs and Au/Al$_2$O$_3$ (3.5nm)/La$_2$O$_3$ (0.4nm)/InGaAs. It is found in Fig. 6(a) that La$_2$O$_3$ is intermixing with InGaAs and that In, Ga and As diffuse deeply into La$_2$O$_3$. Such an intermixing reaction between La$_2$O$_3$ and InGaAs might result in low $D_{it}$ at La$_2$O$_3$/InGaAs.
MOS interfaces [2], while it may also cause a large amount of slow traps in La$_2$O$_3$. It is found in Fig. 6(b) that Al$_2$O$_3$ is intermixing with La$_2$O$_3$ and that Al is diffused through the MOS interface even into InGaAs. As a result, the experimental finding of higher $D_h$ of the sufficiently-thick Al$_2$O$_3$/La$_2$O$_3$/InGaAs interface than that of the La$_2$O$_3$/InGaAs can be explained by the modulation of the La$_2$O$_3$/InGaAs MOS interface due to Al intrusion in the MOS interface.

4. Conclusions

It has been found that the La$_2$O$_3$/InGaAs interfaces provide recorded-low $D_h$ of $\sim 3 \times 10^{11}$ cm$^{-2}$·eV$^{-1}$ as the InGaAs MOS interfaces, while slow traps included in La$_2$O$_3$ cause the large hysteresis. On the other hand, the Al$_2$O$_3$/ultrathin La$_2$O$_3$/InGaAs gate stacks can realize $D_h$ lower than in the conventional Al$_2$O$_3$/InGaAs MOS interfaces with maintaining small hysteresis.

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References


Fig. 1. C-V curves of ALD-deposited La$_2$O$_3$/InGaAs MOS capacitors with La$_2$O$_3$ thickness of (a) 8.2, (b) 2.9 nm La$_2$O$_3$/InGaAs MOS capacitors.

Fig. 2. $D_h$ of 2.9 nm La$_2$O$_3$/InGaAs MOS capacitors.

Fig. 3. C-V curves of Al$_2$O$_3$ (3.5nm)/La$_2$O$_3$/InGaAs gate stacks with the cycle numbers of La$_2$O$_3$ as (a) 0 cycle, (b) 10 cycle (0.4nm) and (c) 40 cycles (2.9nm).

Fig. 4. (a) $D_h$ of the Al$_2$O$_3$ (3.5nm)/La$_2$O$_3$/InGaAs gate stacks as a parameter of the Al$_2$O$_3$ ALD cycle numbers, and (b) the La$_2$O$_3$ ALD cycle number dependence of $D_h$ of Al$_2$O$_3$ (3.5nm)/La$_2$O$_3$/InGaAs at $E - E_c = 0.1$ eV.

Fig. 5. (a) $D_h$ of Al$_2$O$_3$/La$_2$O$_3$ (0.4nm)/InGaAs gate stacks as a parameter of the Al$_2$O$_3$ ALD cycle numbers, and (b) the Al$_2$O$_3$ ALD cycle number dependence of $D_h$ of Al$_2$O$_3$/La$_2$O$_3$ (0.4nm)/InGaAs at $E - E_c = 0.1$ eV.

Fig. 6. TEM image of (a) Au/La$_2$O$_3$ (3.2nm)/InGaAs and (b) Au/Al$_2$O$_3$ (3.5nm)/La$_2$O$_3$ (0.4nm)/InGaAs gate stacks.

Fig. 7. Depth profile of atomic percentages of In, Ga, As, Al and La by EDX analysis of (a) Au/La$_2$O$_3$ (2.9nm)/InGaAs and (b) Au/Al$_2$O$_3$ (3.5nm)/La$_2$O$_3$ (0.4nm)/InGaAs.